# Post-Processing Time-Aware Optimal Scheduling of Single Robotic Cluster Tools

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***Abstract*—Integrated circuit chips are produced on silicon wafers. Robotic cluster tools are widely used since they provide a reconfigurable and efficient environment for most wafer fabrication processes. Recent advances in new semiconductor materials bring about new functionality for integrated circuits. After a wafer is processed in a processing chamber, the wafer should be removed from there as fast as possible to guarantee its high-quality integrated circuits. Meanwhile, maximization of the throughput of robotic cluster tools is desired. This work aims to perform post-processing time-aware scheduling for such tools subject to wafer residency time constraints. To do so, closed-form expression algorithms are derived to compute robot waiting time accurately upon the analysis of particular events of robot waiting for single-arm cluster tools. Examples are given to show the application and effectiveness of the proposed algorithms.**

***Index Terms*—Cluster tool, discrete event systems, optimization, robotic systems, scheduling.**

## I. Introduction

To produce integrated circuit chips, a silicon wafer goes through a great number of fabrication procedures, up to hundreds of steps. Many of these wafer fabrication steps are performed using cluster tools [1], [2]. Typically, four to six processing machines/modules (PM) radially surround a robot to form a cluster tool in a vacuum environment, as illustrated in Fig. 1. The loadlock cassette modules (LL) are used to import/export raw/processed wafers. The robot in the center is responsible for transferring wafers between PMs/LLs. Depending on the number of blades (one or two), a single or dual-arm robot can handle one or two wafers at a time, respectively. The robot unloads a raw wafer from LLs, transfers it to PMs for processing pursuant to a predefined recipe, and returns the completed wafer to LLs [2], [3].

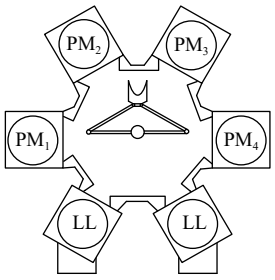


Fig. 1. A single-arm cluster tool.

Cluster tools can perform most wafer fabrication processes, including etching, vapor deposition, wafer cleaning and so on, making them increasingly prevalent in the fabrication processes. Just as done for scheduling complex production systems [4]–[7], much effort has been made on modeling, analysis and scheduling of cluster tools [8]–[24]. Chemical vapor deposition (CVD) used in various wafer fabrication processes require the avoidance of excessive exposure to mixed chemical gases at high temperatures. A wafer thus must be unloaded within a short time from a processing chamber after its processing is completed.

Abundant work has been done for scheduling cluster tools that are subject to such wafer residency time constraints [3], [25]–[29]. In particular, Kim *et al*. [30], Lee and Park [31], and Zuberek [29] have investigated the optimal scheduling problems of dual-arm cluster tools subject to wafer residency time constraints. For cluster tools under such constraints, further work is done in [32]–[35] and analytical-expression-based algorithms are proposed to find periodic optimal schedules whenever a feasible schedule exists. Petri nets have been effectively applied to model cluster tools [32]–[36] and other discrete event systems [37], [38].

A cluster tool starts its operation via a start-up transient process when its robot unloads the first wafer from LLs [39]. Then, it enters the steady state [40], and eventually it undergoes a close-down transient process to terminate its operation when no raw wafers are released from LLs. Yi *et al*. [40] handle the operations under the steady state. Under the steady state, cycle time is referred to as the time taken for finishing a wafer in a repetitive manner [1]. In recent years, due to preferences for small lot production [14], [41], [42] and maintenance demands [43], [44], transient periods including start-up and close-down processes increase to a large proportion during the whole wafer fabrication. The work in

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[45] studies a generalized backward sequence and workload-based conditions to minimize makespan for scheduling such transient processes of single-arm cluster tools with parallel PMs. Kim *et al*. [46] developed latest and earliest starting policies to minimize start-up and close-down periods for dual-arm cluster tools under wafer residency time constraints. For start-up and close-down periods of single-arm cluster tools with wafer residency time constraints, the work in [47]–[49] analyzes schedulability conditions and finds optimal schedules. Kim *et al*. [50] investigate the scheduling problem of start-up and close-down periods for cluster tools subject to task time variation and wafer residency time constraints.

Thanks to significant advancements of semiconductor nanomaterial [51], such as carbon nanotubes and graphene, up-to-date wafer circuit line width has been reduced to less than ten nanometers. As an example, CVD involves a chemical reaction between a mixture of gasses and a wafer's surface that takes place at temperatures up to 1000ºC. For thin line width circuits, there are complex and delicately controllable growth kinetic and reactions to form the circuit layer (s) through CVD. The duration of certain sub-steps has a great influence on the high-quality synthesis of monolayer, bilayer, or few-layer graphene [52]. The quality of devices fabricated on a wafer is heavily dependent on reaction time [51], [53]. Thus, there is an upper-limit with regards to time for which a wafer may stay in a chamber after its processing. If the wafer remains in the chamber past this time limit, it would typically be scrapped. It is crucial to minimize post-processing time for large wafers so that their surfaces absorb fewer by-products in the chamber and can be fabricated uniformly [52]. Therefore, it is desirable to maximize the productivity of wafer fabrication, while minimizing the post-processing time to satisfy the requirement for yielding high-quality circuits.

To the authors' best knowledge, this issue has not been tackled in the literature yet. The main difference between this work and the prior work on scheduling cluster tools is that the latter [3], [10], [13], [54], including our previous work [32], [49], does not consider post-processing time minimization. Since post-processing time minimization and throughput maximization may be in conflict, it can be extremely challenging to find an optimal schedule to optimize both. Furthermore, determining a one-wafer schedule which is simple and easy to understand and implement by practitioners is not obvious. The semiconductor industry prefers one-wafer cyclic scheduling during which after a sequence of robot actions is performed, a cluster tool maintains the exact same state throughout the entire process [10]. Owing to the high capital cost of cluster tools, maximizing throughout is of significant importance in wafer fabrication, we aim to achieve minimization of post-processing time. Despite the scheduling algorithms in prior work which guarantees that post-processing time does not exceed its upper-limit, it is not advised that the post-processing time of a wafer is longer at some steps while it is shorter at other steps because of quality considerations.

This work has twofold contributions: 1) an optimal one-wafer cyclic schedule that maximizes a cluster tool's throughput is found and then the post-processing time is minimized for single-arm cluster tools; and 2) the post-processing time difference among the processing steps is minimized as much as possible. This work proposes algorithms to get an exactly optimal solution in linear-time method instead of a population-based optimization one [55]–[58].

The remainder of this paper is structured as follows. Section II presents the fundamental temporal properties of scheduling single-arm cluster tools. Section III presents algorithms to find a schedule that can minimize cycle time and total post-processing time for single-arm cluster tools. Section IV demonstrates the application of the proposed algorithms. Section V summarizes this work.

## II. Temporal Properties of Single-arm Cluster Tools

With $n$ processing steps in a cluster tool, let $\mathbb{N}_n = \{1, 2, \ldots, n\}$ and $\Omega_n = \{0\} \cup \mathbb{N}_n$. For easy presentation, suppose that each processing step is configured with one PM. For the example shown in Fig. 1, without loss of generality, it is assumed that the wafer processing route is $\langle \mathrm{LL} \rightarrow \mathrm{PM}_1 \rightarrow \mathrm{PM}_2 \rightarrow \mathrm{PM}_3 \rightarrow \mathrm{PM}_4 \rightarrow \mathrm{LL} \rangle$. For single-arm cluster tools, let $\lambda$ and $\mu$ denote the time taken for robot loading/unloading a wafer into/from LLs, and robot moving between any two PMs or between a PM and an LL, respectively. Let $\omega_i$ denote robot waiting time before unloading a wafer from $\mathrm{PM}_i$. If the workload bottleneck is the robot, the cluster tool runs in a transport-bound mode; while if the bottleneck is a PM, it runs in a process-bound mode. Backward scheduling is optimal for the steady state of single-arm cluster tools operating in a process-bound mode [10]. By this scheduling rule, the robot performs the operation sequence as follows:

$\langle$ moving to $\mathrm{PM}_n \rightarrow$ waiting there for $\omega_n$ time units $\rightarrow$ unloading a wafer from $\mathrm{PM}_n \rightarrow$ moving to LLs $\rightarrow$ loading the wafer into LLs $\rightarrow$ moving to $\mathrm{PM}_{n-1} \rightarrow$ waiting there for $\omega_{n-1}$ time units $\rightarrow$ unloading a wafer from $\mathrm{PM}_{n-1} \rightarrow$ moving to $\mathrm{PM}_n \rightarrow$ loading the wafer into $\mathrm{PM}_n \rightarrow$ moving to $\mathrm{PM}_{n-2} \rightarrow$ waiting there for $\omega_{n-2}$ time units $\rightarrow$ unloading a wafer from $\mathrm{PM}_{n-2} \rightarrow \ldots \rightarrow$ unloading a wafer from $\mathrm{PM}_1 \rightarrow \ldots \rightarrow$ moving to LLs $\rightarrow$ waiting there for $\omega_0$ time units $\rightarrow$ unloading a wafer from LLs $\rightarrow$ moving to $\mathrm{PM}_1 \rightarrow$ loading the wafer into $\mathrm{PM}_1 \rightarrow$ moving to $\mathrm{PM}_n$ again$\rangle$.

Let $\alpha_i$ denote the wafer processing time at Step $i$ or $\mathrm{PM}_i$. After a wafer is completed at Step $i$, it cannot stay there for more than $\delta_i$ ($\geq 0$) time units, which is also the upper limit of post-processing time at Step $i$. Some temporal properties of single-arm cluster tools are recalled as follows [32].

The robot cycle time is

$$\psi = 2(n+1)(\lambda+\mu) + \sum_{i=0}^{n} \omega_i = \psi_1 + \psi_2 \tag{1}$$

where the robot's task time $\psi_1 = 2(n+1)(\lambda+\mu)$ is a constant, while $\psi_2 = \sum_{i=0}^{n} \omega_i$ is its waiting time in a cycle.

At Step $i$, the lower bound time required to finish a wafer is

$$\Pi_{iL} = \alpha_i + 4\lambda + 3\mu, \quad i \in \mathbb{N}_n \tag{2}$$

and the upper bound time required to finish a wafer is

$$\Pi_{iU} = \alpha_i + 4\lambda + 3\mu + \delta_i, \quad i \in \mathbb{N}_n. \tag{3}$$

Let $\tau_i$ denote the wafer sojourn time at Step $i$. A wafer should stay in $PM_i$ for $\tau_i \geq \alpha_i$ time to complete its processing, which can be calculated as

$$\tau_i = \psi - (4\lambda + 3\mu + \omega_{i-1}), \quad i \in \mathbb{N}_n. \tag{4}$$

## III. Post-processing Time-aware Scheduling

Let $r_i = \tau_i - \alpha_i$ denote the post-processing time at Step $i$. By (4), it is known that if $\omega_{i-1}$ ($i \in \mathbb{N}_n$) increases, then $r_i$ decreases. The key issue is to minimize the total post-processing time $\sum_{i=1}^{n} r_i$.

For a single-arm cluster tool in a process-bound mode, its lower bound of cycle time is $\Pi = \max\{\Pi_{iL}, i \in \mathbb{N}_n\}$. When a cluster tool operates in a one-wafer cyclic schedule, the robot and all the processing steps operate in a paced way, i.e., $\psi = \Pi$. Our goal is to schedule the robot to achieve its cycle time as $\Pi$ so as to minimize the cycle time for a tool. To avoid violating wafer residency time constraints, schedulability conditions must be established. Upon these conditions, schedules are found to optimize these two objectives. In (1), we have $\psi_2 = \sum_{i=0}^{n} \omega_i$, which implies that if a feasible schedule exists, we must properly assign $\psi_2$ into $\omega_i$, $i \in \Omega_n$, such that the obtained schedule is feasible. When the cycle time is minimal and wafer residency time constraints are satisfied, $\sum_{i=1}^{n} r_i$ must be minimized in order to guarantee high-quality circuits on a wafer. Furthermore, when $\sum_{i=1}^{n} r_i$ is minimized, one must have a uniform substrate across the wafer, or the post-processing time should be evenly distributed among the processing steps. Note that there may be a variety of feasible schedules by assigning $\psi_2$ into $\omega_i$, $i \in \Omega_n$. The optimal one achieves the uniformity among $r_i$'s or $r_i = r_j$, $i, j \in \mathbb{N}_n$. To obtain such a result, we minimize the sum of post-processing time $r_i$'s, which is one of the objectives. In this work, since $\lambda$, $\mu$, and $\alpha_i$'s ($i \in \mathbb{N}_n$) are constants, if $\omega_i$'s are determined, a schedule is found as well.

Based on the above discussion, we propose Algorithm 1 to assign $\psi_2$ into $\omega_i$, $i \in \Omega_n$, so as to obtain a schedule. To calculate a schedule, we must ensure that a feasible schedule exists, since otherwise, it is meaningless. There are two cases where a feasible schedule exists.

*Case 1:* One of the following conditions should be met: 1) $\Pi \leq \Pi_{iU}$ and $\psi_1 \leq \Pi$, $i \in \mathbb{N}_n$; and 2) $\Pi_{iL} \leq \psi_1 \leq \Pi_{iU}$, $i \in \mathbb{N}_n$. Note that $|V|$ denotes the cardinality of set $V$. Condition 1) means that the workloads of all processing step are relatively balanced and the cluster tool is process-bound, while Condition 2 says that the robot is always busy, i.e., the cluster tool is transport-bound.

**Algorithm 1.** Scheduling single-arm cluster tools for Case 1

Input: $\lambda, \mu, \alpha_i, \delta_i$ ($i \in \mathbb{N}_n$)
Output: $\omega_i$ ($i \in \Omega_n$)
1. $\psi_1 \leftarrow 2(n+1)(\lambda + \mu)$
2. $\Pi_{iL} \leftarrow \alpha_i + 4\lambda + 3\mu$ and $\Pi_{iU} \leftarrow \Pi_{iL} + \delta_i$, $i \in \mathbb{N}_n$
3. $\Pi \leftarrow \max\{\Pi_{iL}, i \in \mathbb{N}_n\}$
4. **If** $\Pi \leq \Pi_{iU}$ and $\psi_1 \leq \Pi$, $i \in \mathbb{N}_n$ **Then**
5. $\omega_0 \leftarrow \min\{\Pi - (\alpha_1 + 4\lambda + 3\mu), \Pi - \psi_1\}$
6. $\omega_{i-1} \leftarrow \min\{\Pi - (\alpha_i + 4\lambda + 3\mu), \Pi - \psi_1 - \sum_{k \in \Omega_{i-1} \setminus \{i-1\}} \omega_k\}$ for $i \in \mathbb{N}_n \setminus \{1\}$
7. $\omega_n \leftarrow \Pi - \psi_1 - \sum_{i=0}^{n-1} \omega_i$
8. $r_i \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu + \omega_{i-1})$ for $i \in \mathbb{N}_n$
9. $r_0 \leftarrow \Pi - (4\lambda + 3\mu + \omega_n)$
10. $V \leftarrow \{i |$ ($\Pi_{iL} < \Pi$ and $\omega_{i-1} > 0$) or ($r_i > 0$ and $\omega_{i-1} = 0$), $i \in \mathbb{N}_n\}$
11. **If** ($\omega_n > 0$ and $r_0 = 0$) **Then** $V \leftarrow V \cup \{0\}$ **EndIf**
12. $\Delta \leftarrow \sum_{i \in V} r_i / |V|$
13. **If** $\Delta \leq \Pi - (\alpha_i + 4\lambda + 3\mu)$ and $i \in V$ **Then**
14. **For** each $i \in V$ **do**
15. $r_i \leftarrow \Delta$
16. **If** $i \neq 0$ **Then** $\omega_{i-1} \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu + r_i)$
17. **Else** $\omega_0 \leftarrow \Pi - (\alpha_1 + 4\lambda + 3\mu + r_1)$
18. **EndIf**
19. **EndFor**
20. **EndIf**
21. **EndIf**
22. **If** $\Pi_{iL} \leq \psi_1 \leq \Pi_{iU}$ ($i \in \mathbb{N}_n$) **Then**
23. $\omega_i \leftarrow 0$, for $i \in \Omega_n$
24. **EndIf**

The following result is given to show the optimality of the obtained schedule via Algorithm 1.

*Theorem 1:* For single-arm cluster tools subject to wafer residency time constraints, if one of the two conditions: 1) $\Pi \leq \Pi_{iU}$ and $\psi_1 \leq \Pi$, $i \in \mathbb{N}_n$; and 2) $\Pi_{iL} \leq \psi_1 \leq \Pi_{iU}$, $i \in \mathbb{N}_n$, is satisfied, Algorithm 1 finds a schedule to reach the lower bound of cycle time and minimize total post-processing time.

*Proof:* Set the lower bound $\Pi$ as the cycle time of a cluster tool $\psi = \Pi$, or the minimal cycle time. Next, we check: a) whether a feasible schedule with cycle time $\Pi$ can be constructed or not to meet the residency constraints under one of the given conditions; and b) minimize the post-processing time $\sum_{i=1}^{n} r_i$.

1) Conditions $\Pi \leq \Pi_{iU}$ and $\psi_1 \leq \Pi$, $i \in \mathbb{N}_n$, hold. Since $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1})$, $i \in \mathbb{N}_n$, implying that $\tau_i$ decreases if $\omega_{i-1}$ increases, we need to maximize $\omega_i$'s ($i \in \Omega_n \setminus \{n\}$) so that $\tau_i$ ($i \in \mathbb{N}_n$) can be minimized.

By Line 5 of Algorithm 1, if $\omega_0 = \Pi - (\alpha_1 + 4\lambda + 3\mu) < \Pi - \psi_1$, then $\tau_1 = \Pi - (4\lambda + 3\mu + \omega_0) = \alpha_1$ is minimized and $\tau_1 \in [\alpha_1, \alpha_1 + \delta_1]$. If $\omega_0 = \Pi - \psi_1 < \Pi - (\alpha_1 + 4\lambda + 3\mu)$, $\omega_0$ is maximized because no more time than $\Pi - \psi_1$ can be assigned to $\omega_0$. Then, $\tau_1$ is minimized and $\tau_1 = \Pi - (4\lambda + 3\mu + \omega_0) = \Pi - (4\lambda + 3\mu) - (\Pi - \psi_1) \geq \Pi - (4\lambda + 3\mu) - (\Pi - (\alpha_1 + 4\lambda + 3\mu)) = \alpha_1$, $\tau_1 = \Pi - (4\lambda + 3\mu + \omega_0) \leq \Pi_{1U} - (4\lambda + 3\mu + \omega_0) \leq \Pi_{1U} - (4\lambda + 3\mu) = \alpha_1 + \delta_1$.

By Line 6 of Algorithm 1, if $\omega_{i-1} = \Pi - (\alpha_i + 4\lambda + 3\mu) < \Pi - \psi_1$, then $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1}) = \alpha_i$ is minimized and $\tau_i \in [\alpha_i, \alpha_i + \delta_i]$. If $\omega_{i-1} = \Pi - \psi_1 - \sum_{k \in \Omega_{i-1} \setminus \{i-1\}} \omega_k \leq \Pi - (\alpha_i + 4\lambda + 3\mu)$, $\omega_{i-1}$ is maximized because no more time than $\Pi - \psi_1 - \sum_{k \in \Omega_{i-1} \setminus \{i-1\}} \omega_k$ can be assigned to $\omega_{i-1}$. Then, $\tau_i$ is minimized and $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1}) \geq \Pi - (4\lambda + 3\mu + (\Pi - (\alpha_i + 4\lambda + 3\mu))) = \alpha_i$, and $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1}) \leq \Pi_{iU} - (4\lambda + 3\mu + \omega_{i-1}) = \alpha_i + \delta_i - \omega_{i-1} \leq \alpha_i + \delta_i$.

Thus, wafer residency constraints are satisfied when $\omega_i$ ($i \in \Omega_n$) is set by Lines 5–7 of Algorithm 1 while $\sum_{i=1}^{n} r_i$ is minimized. Then, Lines 8–20 intend to readjust the post-processing time evenly for Steps in $V = \{i | (\Pi_{iL} < \Pi$ and $\omega_{i-1} > 0)$ or $(r_i > 0$ and $\omega_{i-1} = 0)$, $i \in \mathbb{N}_n\}$. Furthermore, during the

adjustment process, $\sum_{i=1}^{n} r_i$ keeps unchanged.

If $\Delta \le \Pi - (\alpha_i + 4\lambda + 3\mu)$ ($i \in V$) holds in Line 13, then, by Lines 16 and 17, we have $\omega_{i-1} = \Pi - (\alpha_i + 4\lambda + 3\mu + \Delta) \ge \Pi - (\alpha_i + 4\lambda + 3\mu + \Pi - (\alpha_i + 4\lambda + 3\mu)) = 0$ ($i \ne 0$) and $\omega_0 = \Pi - (\alpha_1 + 4\lambda + 3\mu + \Delta) \ge \Pi - (\alpha_i + 4\lambda + 3\mu + \Pi - (\alpha_i + 4\lambda + 3\mu)) = 0$. Obviously, for $i \in V$, $r_i = \Delta > 0$ and $r_i = \Delta \le \Pi - (\alpha_i + 4\lambda + 3\mu) \le \Pi_{iU} - (\alpha_i + 4\lambda + 3\mu) = \delta_i$.

2) Condition $\Pi_{iL} \le \psi_1 \le \Pi_{iU}$ ($i \in \mathbb{N}_n$) holds as shown in Line 22 in Algorithm 1, we have $\omega_i = 0$, $i \in \Omega_n$. Then, $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1}) = \Pi - (4\lambda + 3\mu) \ge \Pi_{iL} - (4\lambda + 3\mu) = \alpha_i$, $\tau_i = \Pi - (4\lambda + 3\mu) \le \Pi_{iU} - (4\lambda + 3\mu) = \alpha_i + \delta_i$.

So far, we can conclude that if one of the given conditions in this theorem is satisfied, Algorithm 1 can find a schedule that minimizes both the cycle time and wafer post-processing time. ■

By Lines 5–7, Algorithm 1 initially finds a schedule with both cycle time and wafer post-processing time being minimized. Lines 8–20 make efforts to readjust post-processing time evenly for some steps. This adjustment can avoid unnecessarily excessive post-processing time, which is beneficial in improving the quality of the fabricated wafer.

In Algorithm 1, all the statements make calculations based on closed-form expressions. The number of iterations in the For-loop of Lines 14–19 cannot be greater than $n$. It is obvious that the computational complexity of Algorithm 1 is $O(n)$.

*Case 2:* $\bigcap_{k\in\mathbb{N}_n} [\Pi_{kL}, \Pi_{kU}] = \emptyset$, which implies that the workloads of the processing steps are unbalanced. In this case, Algorithm 2 is proposed to determine whether a feasible schedule can be found, and whether the lower bound of cycle time of the found schedule is reached.

**Algorithm 2.** Scheduling single-arm cluster tools for Case 2

Input: $\lambda, \mu, \alpha_i, \delta_i$ ($i \in \mathbb{N}_n$)
Output: $\Gamma, \omega_i$ ($i \in \Omega_n$)
1. $\Gamma \leftarrow$ True, $\psi_1 \leftarrow 2(n+1)(\lambda + \mu)$
2. $\Pi_{iL} \leftarrow \alpha_i + 4\lambda + 3\mu$, $\Pi_{iU} \leftarrow \Pi_{iL} + \delta_i$, $i \in \mathbb{N}_n$
3. $\Pi \leftarrow \max\{\Pi_{iL}, i \in \mathbb{N}_n\}$
4. $E \leftarrow \{k | \Pi_{kU} < \Pi, k \in \mathbb{N}_n\}$, $F \leftarrow \mathbb{N}_n \setminus E$
5. $\omega_{i-1} \leftarrow \Pi - (\alpha_i + \delta_i + 4\lambda + 3\mu)$, for $i \in E$
6. $\omega_{i-1} \leftarrow 0$, for $i \in F$
7. **If** $\sum_{i\in E} \omega_{i-1} > \Pi - \psi_1$ **Then**
8. $\Gamma \leftarrow$ False, return //Unschedulable.
9. **EndIf**
10. $G \leftarrow \{i | i \in F$ and $\Pi_{iL} < \Pi\}$
11. $\omega_{i-1} \leftarrow 0$, $i \in F \setminus G$
12. $\psi \leftarrow \Pi - \psi_1 - \sum_{i\in E} \omega_{i-1}$
13. $h \leftarrow \sum_{i\in G} (\Pi - (\alpha_i + 4\lambda + 3\mu))$
14. **If** $\psi > h$ **Then**
15. $\omega_{i-1} \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu)$, $i \in G$
16. $\omega_n \leftarrow \psi - h$
17. $r_i \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu + \omega_{i-1})$ for $i \in \mathbb{N}_n$
18. **Else**
19. $\Upsilon \leftarrow h - \psi$, $H \leftarrow G$
20. $\omega_n \leftarrow 0$
21. **Do**
22. $A \leftarrow \{i | i \in H$ and $\Upsilon/|H| > \Pi - (\alpha_i + 4\lambda + 3\mu)\}$
23. **If** $A \ne \emptyset$ **Then**
24. $r_i \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu)$, $i \in A$
25. $\omega_{i-1} \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu + r_i)$, $i \in A$
26. $\Upsilon \leftarrow \Upsilon - \sum_{i\in A} r_i$, $H \leftarrow H \setminus A$
27. **If** $\Upsilon < 0$ **Then** goto Adjust **EndIf**
28. **Else**
29. $r_i \leftarrow \Upsilon/|H|$, $i \in H$
30. $\omega_{i-1} \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu + r_i)$, $i \in H$
31. $\Upsilon \leftarrow \Upsilon - \sum_{i\in H} r_i$
32. $H \leftarrow \emptyset$
33. **EndIf**
34. **While** $H \ne \emptyset$
35. **If** $\Upsilon < 0$ **Then**
36. **Adjust:** $\psi_G \leftarrow 0$
37. **For** $i \in G$
38. $\omega_{i-1} \leftarrow \min\{\Pi - (\alpha_i + 4\lambda + 3\mu), \psi - \psi_G\}$
39. $r_i \leftarrow \Pi - (\alpha_i + 4\lambda + 3\mu + \omega_{i-1})$
40. $\psi_G \leftarrow \psi_G + \omega_{i-1}$
41. **EndFor**
42. **EndIf**
43. **EndIf**

*Theorem 2:* If $\bigcap_{k\in\mathbb{N}_n} [\Pi_{kL}, \Pi_{kU}] = \emptyset$, Algorithm 2 can determine whether a feasible schedule exists. If it does, Algorithm 2 can find a schedule that minimizes both the cycle time and post-processing time.

*Proof:* By Line 4 of Algorithm 2, we have $E = \{k | \Pi_{kU} < \Pi, k \in \mathbb{N}_n\}$. For Steps $i \in E$, since the cycle time of every step must be identical to obtain a one-wafer cyclic schedule, $\omega_i$'s ($i \in E$) must be set by Line 5, which means that $\omega_i$'s ($i \in E$) have been maximized. Thus, by $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1})$, $\tau_i$ 's ($i \in E$) are minimized.

If $\sum_{i\in E} \omega_{i-1} \le \Pi - \psi_1$ holds, it is feasible to find a schedule by Lines 5 and 6. If not, there is no feasible schedule as specified by Lines 7–9.

Lines 4 and 10 define that $F = \mathbb{N}_n \setminus E$ and $G = \{i | i \in F$ and $\Pi_{iL} < \Pi\}$. For Steps $i \in F \setminus G$, we have $\Pi_{iL} = \Pi$. By Line 11, $\omega_{i-1} = 0$, then $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1}) = \Pi - (4\lambda + 3\mu) = \Pi_{iL} - (4\lambda + 3\mu) = \alpha_i \in [\alpha_i, \alpha_i + \delta_i]$ and $r_i = \tau_i - \alpha_i = 0$ is minimized.

Next, check if $r_i$ ($i \in G$) is minimized and the residency time constraints for Steps 1–$n$ are satisfied. Lines 12 and 13 set $h = \sum_{i\in G} (\Pi - (\alpha_i + 4\lambda + 3\mu))$ and $\psi = \Pi - \psi_1 - \sum_{i\in E} \omega_{i-1}$. There are two cases which are discussed below.

*Case A:* $\psi > h$.

By Line 15, for Steps $i \in G$, $\omega_{i-1} = \Pi - (\alpha_i + 4\lambda + 3\mu)$, then $\tau_i = \Pi - (4\lambda + 3\mu + \omega_{i-1}) = \alpha_i \in [\alpha_i, \alpha_i + \delta_i]$ and $r_i = \tau_i - \alpha_i = 0$ is minimized. Hence, $r_i$ is minimized for Steps $i \in F$.

*Case B:* $\psi \le h$.

Lines 4, 12, 20, and 22 of Algorithm 2 present that $A = \{i | i \in H$ and $\Upsilon/|H| > \Pi - (\alpha_i + 4\lambda + 3\mu)\}$, implying that $\Pi_{iL} < \Pi \le \Pi_{iU}$ and $\Upsilon/|H| > \Pi - (\alpha_i + 4\lambda + 3\mu)$.

If $A \ne \emptyset$, i.e., $\Upsilon/|H| > \Pi - (\alpha_i + 4\lambda + 3\mu)$, then by Lines 24 and 25, we have $\omega_{i-1} = \Pi - (\alpha_i + 4\lambda + 3\mu + \Pi - (\alpha_i + 4\lambda + 3\mu)) = 0$ for Steps $i \in A$. Thus, by Line 24, $r_i = \Pi - (\alpha_i + 4\lambda + 3\mu) \ge \Pi_{iL} - (\alpha_i + 4\lambda + 3\mu) = 0$, $r_i \le \Pi_{iU} - (\alpha_i + 4\lambda + 3\mu) = \delta_i$. By Line 27, if $\Upsilon > 0$, i.e., there are $\Upsilon$ time units that can be assigned to the post-processing time at the steps in $H$. If $\Upsilon < 0$ holds, then it leads to a contradictory as follows. If $\Upsilon < 0$, then $h - \psi - \sum_{i\in G\setminus H} r_i < 0$, or $\sum_{i\in G\setminus H} r_i > h - \psi$. If Line 27 is removed and all $\omega_{i-1}$'s ($i \in G$) are set by this "do-while" loop in Lines 21–34, then $\sum_{i\in G} \omega_{i-1} = \sum_{i\in G} \Pi - (\alpha_i + 4\lambda + 3\mu + r_i) = \sum_{i\in G} (\Pi - (\alpha_i +$

$4\lambda+3\mu)) - \sum_{i\in G} r_i = h - \sum_{i\in G} r_i$. Equation (1) and Lines 11, 12 and 20 imply $\sum_{i\in G} \omega_{i-1} = \psi$. Thus, $\sum_{i\in G} r_i = h - \psi$, which is contradictory to the aforementioned $\sum_{i\in G\setminus H} r_i > h - \psi$ because of $\sum_{i\in \mathrm{H}} r_i > 0$. Thereby, if $\Upsilon < 0$ occurs in Line 27, Lines 36–41 can reset $\omega_{i-1}$'s ($i \in G$). By Line 38, if $\omega_{i-1} = \Pi - (\alpha_i + 4\lambda + 3\mu) < \psi - \psi_G$, then $r_i = \Pi - (\alpha_i + 4\lambda + 3\mu + \omega_{i-1}) = 0$ is minimized. By Line 38, if $\psi - \psi_{\mathrm{G}} < \Pi - (\alpha_i + 4\lambda + 3\mu)$, then there are $\psi - \psi_{\mathrm{G}}$ time units available to be assigned to $\omega_{i-1}$, or $\omega_{i-1} = \psi - \psi_{\mathrm{G}}$ is maximized. Then, $r_i = \Pi - (\alpha_i + 4\lambda + 3\mu + \omega_{i-1}) = \Pi - (\alpha_i + 4\lambda + 3\mu + \psi - \psi_G) > \Pi - (\alpha_i + 4\lambda + 3\mu + (\Pi - (\alpha_i + 4\lambda + 3\mu))) = 0$ and $r_i = \Pi - (\alpha_i + 4\lambda + 3\mu + \psi - \psi_G) \le \Pi - (\alpha_i + 4\lambda + 3\mu + 0) \le \Pi_{iU} - (\alpha_i + 4\lambda + 3\mu) = \delta_i$ because of $\psi - \psi_G \ge 0$.

If $A = \emptyset$ does not hold, then $\Upsilon/|H| \le \Pi - (\alpha_i + 4\lambda + 3\mu)$. This situation is handled by Lines 29–32, distributing post-processing time evenly. By Lines 29 and 30, for Steps $i \in H$, $\omega_{i-1} = \Pi - (\alpha_i + 4\lambda + 3\mu + \Upsilon/|H|)$, $r_i = \Upsilon/|H| \le \Pi - (\alpha_i + 4\lambda + 3\mu) \le \Pi_{iU} - (\alpha_i + 4\lambda + 3\mu) = \delta_i$. After Lines 29–32 are executed only once, $\Upsilon$ becomes zero and $H$ becomes $\emptyset$. This means that the condition $\Upsilon < 0$ in Line 35 cannot be met.

So far, for $i \in E \cup F$, we have $\sum_{i\in E\cup F} \omega_{i-1} = \sum_{i\in E} \omega_{i-1} + \sum_{i\in G} \omega_{i-1} + \sum_{i\in F\setminus G} \omega_{i-1} = \sum_{i\in E} \omega_{i-1} + (\Pi - \psi_1 - \sum_{i\in E} \omega_{i-1}) + 0 = \Pi - \psi_1$. Meanwhile, $\omega_n$ has been set to be zero by Line 20. ■

Algorithm 2 deals with the situation of $\bigcap_{k\in\mathbb{N}_n} [\Pi_{kL}, \Pi_{kU}] = \emptyset$ which indicates that some steps have heavier workloads than others. Given the lower bound of cycle time, robot waiting time $\omega_{i-1}$ ($i \in E$) is assigned in advance. After its assignment, one can decide if the cluster tool is schedulable as done in Line 7. Then we compare the workload of the robot with those of the processing steps, and if the robot is fast enough, the post-processing time can be minimized to be zero, which is implemented in Lines 15–17. If not, there is non-zero post-processing time for Steps $i \in G$. Then, the sum of them, i.e., $\sum_{i\in G} r_i$ is minimized and $r_i$ ($i \in E$) is set evenly, as implemented in Lines 19–42.

In Algorithm 2, all the statements make calculations based on closed-form expressions. The count of iterations in Lines 21–34 and 37–41 cannot be greater than $n$. It is obvious that the computational complexity of Algorithm 2 is $O(n)$.

## IV. Examples

In this section, we demonstrate how to apply the proposed method to find schedules for bi-objective problems. The time unit is seconds and is omitted thereafter. Let $(r'_1, r'_2, r'_3, r'_4)$ denote the post-processing time if a cluster tool is scheduled by a conventional method that does not consider minimizing the post-processing time.

*Example 1:* There are four steps in a single-arm cluster tool where every step is equipped with one PM. The robot waiting time is found by Algorithm 1. The activity time, wafer residency time constraints and the post-processing time at each step (excluding Step 0 or LLs) is given as follows:

$$(\alpha_1, \alpha_2, \alpha_3, \alpha_4; \lambda, \mu) = (50, 66, 52, 50; 4, 2)$$
$$(\delta_1, \delta_2, \delta_3, \delta_4) = (20, 20, 20, 20)$$
$$(\omega_0, \omega_1, \omega_2, \omega_3, \omega_4) = (10, 0, 8, 10, 0)$$
$$(r_1, r_2, r_3, r_4) = (6, 0, 6, 6), \sum_{i=1}^{4} r_i = 18.$$

If the existing algorithms in [32] are applied to find an optimal schedule, we obtain post-processing time as $(r'_1, r'_2, r'_3, r'_4) = (16, 0, 14, 16)$ and $\sum_{i=1}^{4} r'_i = 46$. By our algorithm, the total post-processing time is decreased by 60.9%. Furthermore, $r_i$, $i \in \mathbb{N}_4$, is evenly distributed among the four steps.

The schedules obtained by Algorithm 1 and previous work in [32] are shown by Gantt charts in Fig. 2. The post-processing time is indicated by red bars in Figs. 2–4.

*Example 2:* There are four steps in a single-arm cluster tool where every step is equipped with one PM. It satisfies $\bigcap_{k\in\mathbb{N}_4} [\Pi_{kL}, \Pi_{kU}] = \emptyset$. The schedulability condition $\sum_{i\in E} \omega_{i-1} \le \Pi - \psi_1$ holds. Thus, the robot waiting time are found by Algorithm 2. The activity time, wafer residency time constraints, and the post-processing time at each step (excluding Step 0 or LLs) are

*Case 1:* $\psi > h$.

$$(\alpha_1, \alpha_2, \alpha_3, \alpha_4; \lambda, \mu) = (85, 120, 110, 85; 5, 2)$$
$$(\delta_1, \delta_2, \delta_3, \delta_4) = (20, 20, 20, 20)$$
$$(\omega_0, \omega_1, \omega_2, \omega_3, \omega_4) = (15, 0, 10, 15, 36)$$
$$(r_1, r_2, r_3, r_4) = (20, 0, 0, 20), \sum_{i=1}^{4} r_i = 40.$$

If the algorithms in [32] are applied to find an optimal schedule, we have $(r'_1, r'_2, r'_3, r'_4) = (20, 0, 10, 20)$ and $\sum_{i=1}^{4} r'_i = 50$. The total post-processing time is decreased by 20%. The schedules obtained by Algorithm 2 and previous work in [32] are shown by Gantt charts in Fig. 3.

*Case 2:* $\psi < h$.

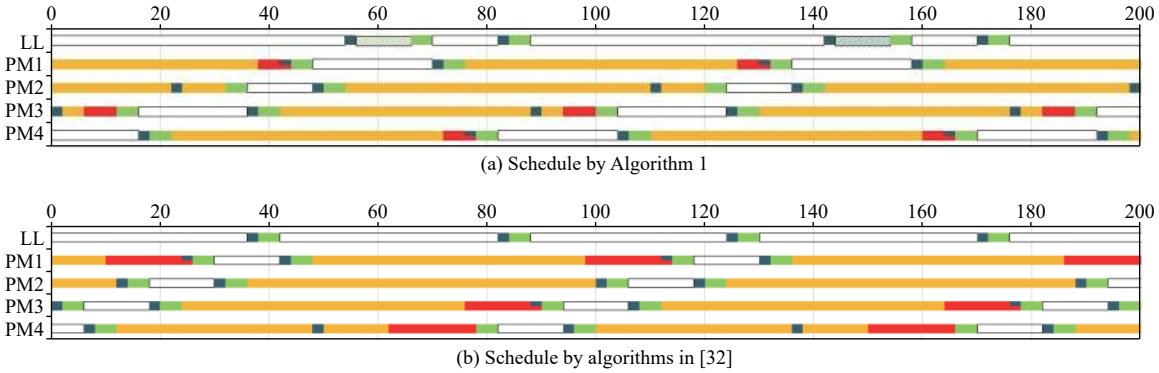
$$(\alpha_1, \alpha_2, \alpha_3, \alpha_4; \lambda, \mu) = (36, 80, 78, 66; 4, 2)$$
$$(\delta_1, \delta_2, \delta_3, \delta_4) = (10, 10, 3, 14)$$
$$(\omega_0, \omega_1, \omega_2, \omega_3, \omega_4) = (34, 0, 0, 8, 0)$$
$$(r_1, r_2, r_3, r_4) = (10, 0, 2, 6), \sum_{i=1}^{4} r_i = 18.$$

The algorithms in [32] find an optimal schedule with $(r'_1, r'_2, r'_3, r'_4) = (10, 0, 2, 14)$ and $\sum_{i=1}^{4} r'_i = 26$. The total post-processing time is decreased by 30.8%. The schedules obtained by Algorithm 2 and previous work in [32] are shown by Gantt charts in Fig. 4.

We conclude that the proposed algorithms can find the same optimal-cycle-time schedule as the existing ones [32] but with significantly reduced post-processing time.

## V. Conclusions

Cluster tools are extensively adopted for wafer fabrication equipment in the semiconductor manufacturing industry. Wafers are fabricated in a complex chemical reaction environment where there are mixed gases and high-temperature heat. Characteristics of new materials and high-quality chips require that after their processing is completed, they should leave the processing chamber as soon as possible. The existing research ensures that post-processing time does not exceed the upper limit only. In order to obtain high-quality integrated circuits with advanced process control, this work considers two optimization objectives for single-arm cluster

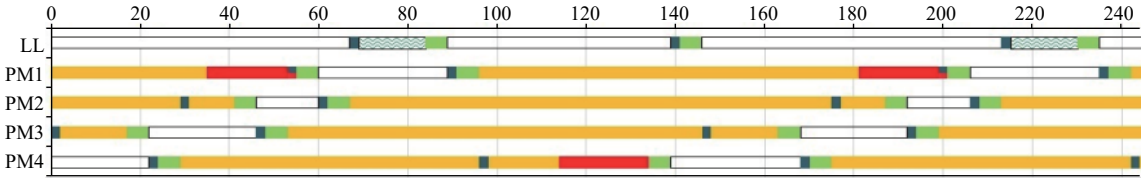



(a) Schedule by Algorithm 1

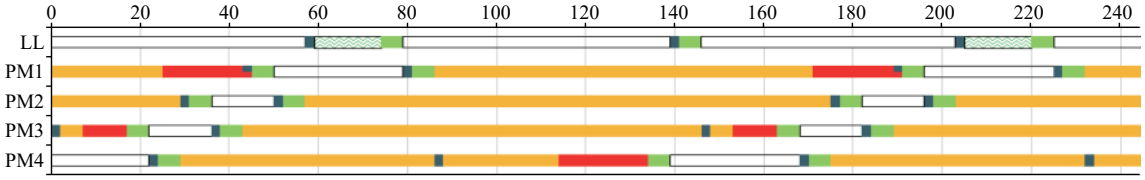



(b) Schedule by algorithms in [32]

Fig. 2. Gantt chart for Example 1.

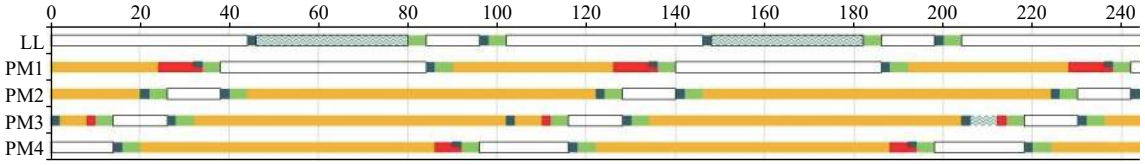



(a) Schedule by Algorithm 2

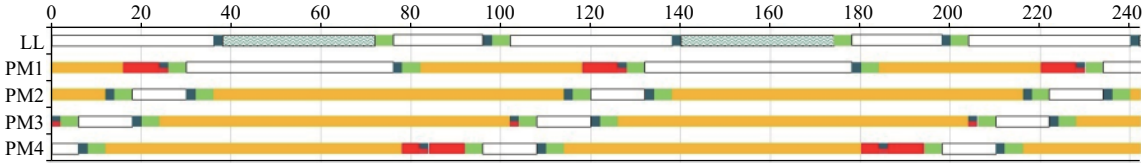



(b) Schedule by algorithms in [32]

Fig. 3. Gantt chart for Case 1 of Example 2.




(a) Schedule by Algorithm 2




(b) Schedule by algorithms in [32]

Fig. 4. Gantt chart for Case 2 of Example 2.

tools subject to wafer residency time constraints. It not only considers the maximization of the throughput but also minimizes wafer post-processing time in processing chambers. When the throughput is maximized and wafer residency time constraints are satisfied, we make efforts to shorten wafer sojourn time after a wafer is processed to avoid uneven post-processing time among the processing steps. Therefore, the obtained schedules are significantly better for fabricating high-quality wafers which are not seen in the existing reports to our best knowledge. In the future, we intend to answer how to schedule multi-cluster tools with multiple optimization goals.

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