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3D integration review

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Abstract 3-D integration delivers value by increasing the volumetric transistor density with the potential benefit of shorter electrical path lengths through use of the shorter third dimension. Several researchers have studied various aspect of 3Di such as bonding level, through silicon via processes and integration, thermo-mechanical reliability of the vias, and the impact of the vias on devices. In this paper, we review some of the literature with a view to understanding the key options and challenges in 3Di. We also discuss some important applications of this technology, and the constraints that have to be overcome to make it work.

Keywords 3D integration, embedded memory, through silicon via, die stacking

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1 Introduction

Three dimensional integration of circuits is an attractive approach to stay on the semiconductor productivity roadmap. Briefly, the principal value of 3D integration lies in increasing the volumetric transistor density with the potential benefit of shorter electrical path lengths through use of the shorter third dimension. An additional advantage is the intimate integration of disparate technologies such as power amplifiers with digital CMOS. However, as we study this problem in some detail we uncover a serious set of constraints especially for high performance applications. These constraints can be classified in four broad categories: the overhead and design constraints of through silicon vias (TSVs); power delivery and distribution in multiple strata; heat dissipation across the 3D stack; and finally reparability of the 3D stack. In this paper we will examine these constraints in detail based on our experience with high end processors. We begin with a review of the literature including a discussion of the various flavors of 3D implementation and then address some of the constraints referred to above.

A recent analysis of IBM's z196 mainframe by Morgan [1] shows that having more memory closer to the chip is more important than having fast memory. In other words, super processors are increasingly being limited by the speed of access to memory. Most multi chip module designs are arranged to enable the CPU (central processor unit) to readily communicate with a variety of cache memory on the module. The z196 CPU has 24 MB of eDRAM (embedded dynamic random access memory) L3 cache memory, which splits into two banks. However, to fully leverage the power of such a CPU, cache memory must be provided with much shorter access paths. The only way out is to travel in the z-direction, i.e. vertically. This memory integration is certainly one prime driver for 3D integration.

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In 2005, Zeng et al. [2] used a simulator based on analytical models to build processor-memory configurations for both a graphics processor and a microprocessor. They showed that 3D design was useful in reducing the length of many global interconnects without introducing logic complexity. They concluded that with micron-sized inter wafer vias, 3D integration at the wafer level, delivered a large memory bandwidth without forsaking too much silicon real estate. In 2006, Black et al. [3] modeled two die combinations of memory+logic, and logic+logic in face to face joining through dense via interconnects. They were able to show that a 32 MB 3D stacked DRAM cache can reduce the cycles per memory access of a two-threaded RMS benchmark significantly, while increasing peak temperature by a negligible amount. Other studies have shown similar results, i.e. 3D stacking of die has performance advantages that make it not only a very attractive architectural proposition, but also a requirement as we approach situations where memory accessibility becomes the gate for CPU performance.

2 Current status

3Di (three-dimensional integration) refers to a family of technologies which enable the stacking of active Si layers with vertical connections between them. Fundamentally there are two approaches for 3D stacking: bonding silicon at the wafer level or joining it at the die level (which includes die to die and die to wafer bonding). Each of these approaches comes with advantages as well as limitations. Within each type of bonding method, there is an option of joining which enables dies to either face each other, i.e. F2F (Face to Face), or one die to be joined to the back of the other, i.e. F2B (Face to Back). However, much of the reported work has concentrated on the F2F approach. It is important to note that 3D stacking generally encompasses both silicon level stacking and packaging level stacking. Reviews of the various types of 3D stacking, and their advantages, may be found in recent publications [4–9].

2.1 W2W (wafer to wafer) bonding

Wafer to wafer bonding typically involves joining wafers either by metallic or oxide bonds. An example of wafer to wafer bonding is shown in Figure 1 [10]. Joining often precedes wafer thinning and final wiring on the thinned wafer backside. Wafer to wafer bonding is uniquely suited to fine pitch applications in the range of 1–10 μm. This approach requires the same die size on both wafers, and is most practical if both wafers have relatively high yields. If thinning is done after bonding, a temporary carrier is not required, which eliminates the process steps associated with carrier attachment and removal. If thinning is done prior to bonding, it will necessitate the use of a temporary carrier. Ohba [11] has discussed both types of wafer bonding methods, i.e. thinning before bonding, and via-last after bonding, and performed estimation of yields for 4-wafer stacking.

In either case, however, large variations in topography of the finished wafers can severely limit the use of wafer to wafer bonding.

Typical methods for wafer to wafer bonding include solid state metallic bonding and oxide fusion bonding. In solid state metal bonds, attachment of two wafers is achieved using pressure at elevated temperatures, in order to create local joints between copper features on two opposing surfaces. Optimization of this process is critical to ensure a high quality bond. A variation of the copper to copper thermo-compression bond is the transfer-join assembly process [10]. In this method, the mating surfaces are provided with complementary features, such that one side has protrusions whereas the other side has receiving wells. An adhesive layer may also be used to improve the bond characteristics, by flowing and thereby filling any gaps in the bonded structures. Refer to Figure 2 [10].

Oxide fusion bonding is yet another method that is employed for permanently bonding two wafers together. In 2005, Topol et al. [12] described in detail the process for SOI (silicon on insulator)-based assembly for 3D integrated circuits. This technique requires a low temperature oxide deposition followed by appropriate surface activation to prepare the wafers for bonding. Extreme planarization of the opposing surfaces is generally a requirement [13]. Work has also been performed to study the effect of UV (ultra-violet) annealing of the oxide films prior to bonding [9]. One of the key issues in oxide fusion bond-

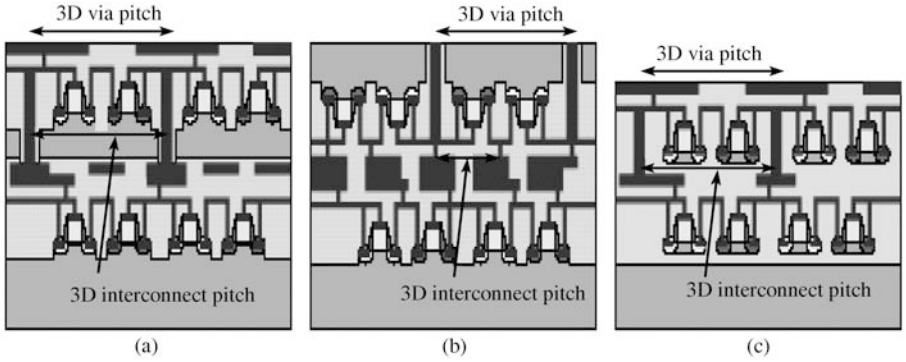

Figure 1 Example of wafer to wafer bonding [10].

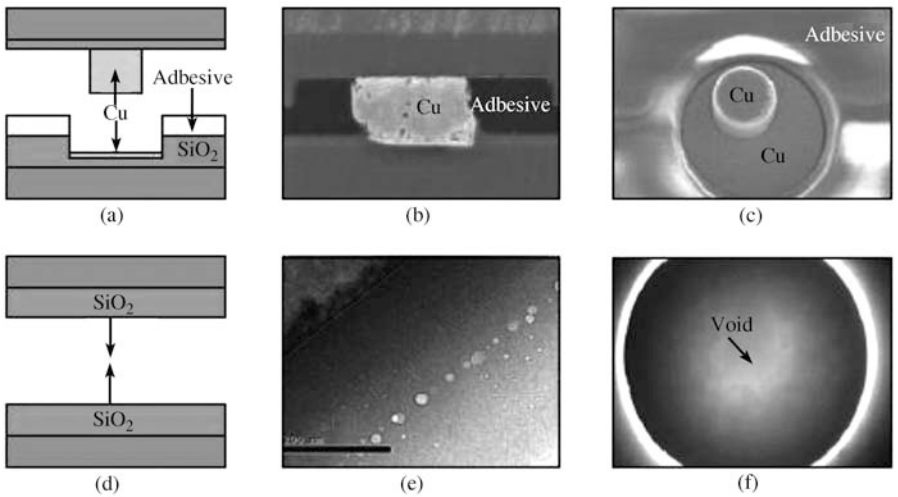

Figure 2 Adhesive layer method for W2W bonding [10].

ing is the presence of micro-voids which have the propensity to coalesce and move towards the interface, creating a weakness in the resultant structure. Hence, a closely monitored process with the correct surface treatments and bonding conditions is needed to result in a strong final bond. A schematic of a 3D structure joined by oxide fusion bonding is shown in Figure 3 [10]. A variation on oxide bonding is a room temperature direct oxide bond process developed by Ziptronix [14].

Variations on W2W thermo-compression bonding may involve the use of a polymer such as BCB at the interfaces of interest, resulting in a hybrid Cu-Cu thermo-compression bond [15–17]. Researchers have been able to show that such hybrid bonding can result in yields of 96% for structures with 10 μm pitch TSV's [16]. Others have shown that when a true via-last process is used, stacks comprising as many as 7 wafers may be successfully joined to each other, and connected with the use of TSV's [11].

The handling of thinned wafers is an essential component of wafer to wafer bonding when thinning occurs prior to wafer bonding. To tackle this challenge, work has been done to develop WSS (wafer support systems), in which the thinned wafers are temporarily bonded to a carrier wafer to give it mechanical stability [18]. Another approach is to use a carrier-less system in which the wafer is modified in a way as to give it mechanical rigidity despite being thin [19].

2.2 D2D (die to die) bonding

Die to die bonding has a much lower throughput than wafer to wafer bonding, but it is not limited by differences in die size, wafer size, or yield on individual wafers. This method can be used to join KGD (known good die) after testing, thus ensuring higher yield after final assembly. Figure 4 depicts a 6-layer chip stack; Figure 5 represents a cross-sectional SEM image of a similar chip stack showing individual die joined by lead-free solder interconnect [20].

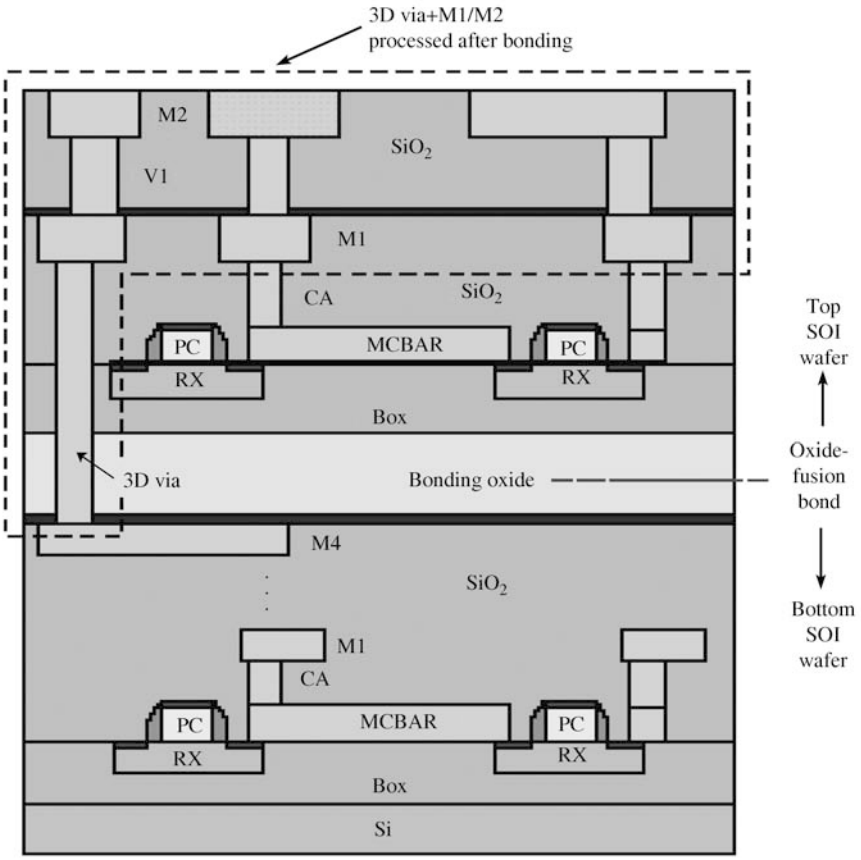

Figure 3 Wafers joined by oxide fusion bonding [10].

Die to die bonding has the advantage of being less sensitive to topographical variations across wafer surfaces, since the bonding area is considerably smaller than in wafer to wafer joining. Further, this method does not affect the essential silicon fabrication method, since there is no bonded wafer pair to thin, and process. However, this approach needs a temporary handler because the silicon is typically thinned to below 100 μm, before it is joined. Also, the die to die or die to wafer bonding approach may more closely resemble standard chip assembly practices.

Although KGD are desired for high assembly yield, it may not always be possible to do complete testing at the wafer level. This necessitates the development of a process for the temporary attachment of chips, which is particularly valuable in 3D stacking. Figure 6 [21] shows an SEM image of a reworked chip stack on a TCA (temporary chip attach) substrate, after testing. The authors have shown that a rework process can be successfully implemented using a hot shear method to detach the chip from the TCA, and then prepare it for joining to the final substrate [21].

Another key difference between wafer level bonding and die level bonding is the depth of the TSV (through silicon via). In wafer level bonding, the TSV is typically constructed after the wafers are bonded and the top wafer is thinned. Because the thinned wafer is continuously supported by the thicker wafer to which it is bonded, this thinned wafer can be reduced to a final thickness of 10 μm without any issue. The TSV that is subsequently formed is therefore also ∼10 μm deep. In contrast, for die level bonding, the TSV is typically constructed in the wafer prior to thinning. The handling issues associated with the final thinned wafer place limits on how thin the wafer can get. This thickness is typically 50–100 μm. The TSV depth is therefore also typically in that regime. Due to aspect ratio limits for TSV's, it naturally follows that TSV's in wafer level bonding can therefore be smaller in diameter and more tightly packed than those in die level bonding.

2.3 D2W (die to wafer) bonding

Yet another method that has its proponents is die to wafer bonding in which multiple die are placed on a

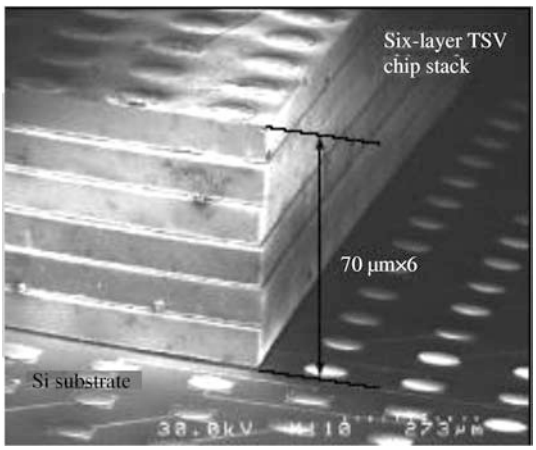

Figure 4 Six-layer chip stack [20].

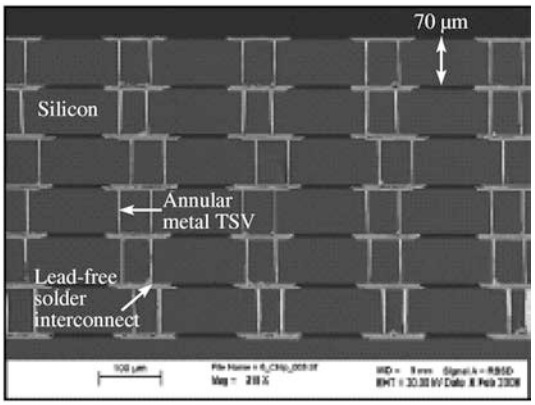

Figure 5 SEM image of stacked die [20].

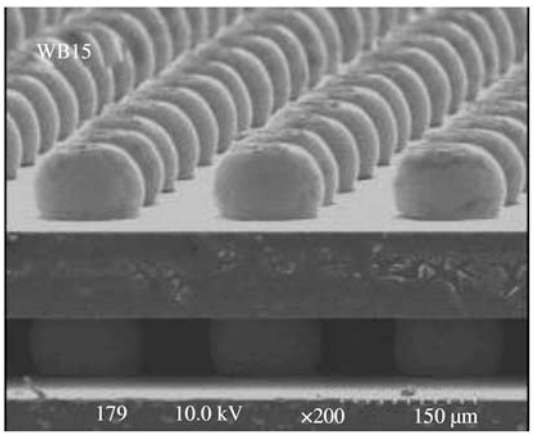

Figure 6 SEM image of a reworked chip stack [20].

wafer and then joined simultaneously. This gives a tremendous advantage in two respects: the use of KGD, and the efficiency gained by doing gang bonding. However, planarization of the stacked die is mandated for the successful use of this method. A process whereby the landing wafer is populated with KGD on top containing TSV's, is described by Van Olmen et al. [22]. Validation of the industrial compatibility of a high density TSV process to the D2W bond and planarization method has been described by Leduc et al. [23].

2.4 TSV integration

A key factor in any type of 3D integration is the introduction of TSV's in the fabrication sequence. For wafer to wafer bonding, TSV's may be introduced after bonding and thinning. This is an example of a via-last process. If, however, TSV's are introduced in the wafers prior to bonding, it would result in a via-first process. For die to die bonding, or die to wafer bonding, the TSV's must be introduced in the silicon long before the die are bonded. If the TSV's are introduced very early in the fabrication sequence, before the devices are built, this would be termed a via-first process. However, for several reasons, including TSV form factor and choice of metallization, it may be more prudent to introduce TSV's during the BEOL (back end of line) fabrication, i.e. a via-middle process. It is to be noted that the point of introduction of the TSV plays a critical role in the choice of TSV processes, including materials and temperatures used.

2.5 TSV processes

The TSV process comprises the following steps: via etching, via insulation, deposition of the diffusion barrier/liner/seed, deposition of the metal/alloy to completely or partially fill the TSV, deposition of any

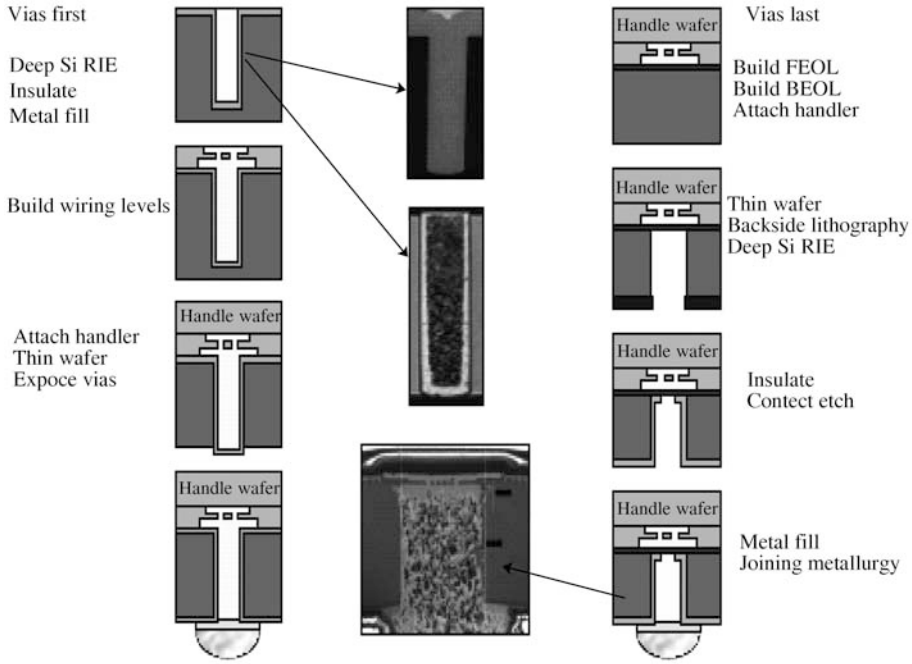

Figure 7 Comparison of via first and via last processes [24].

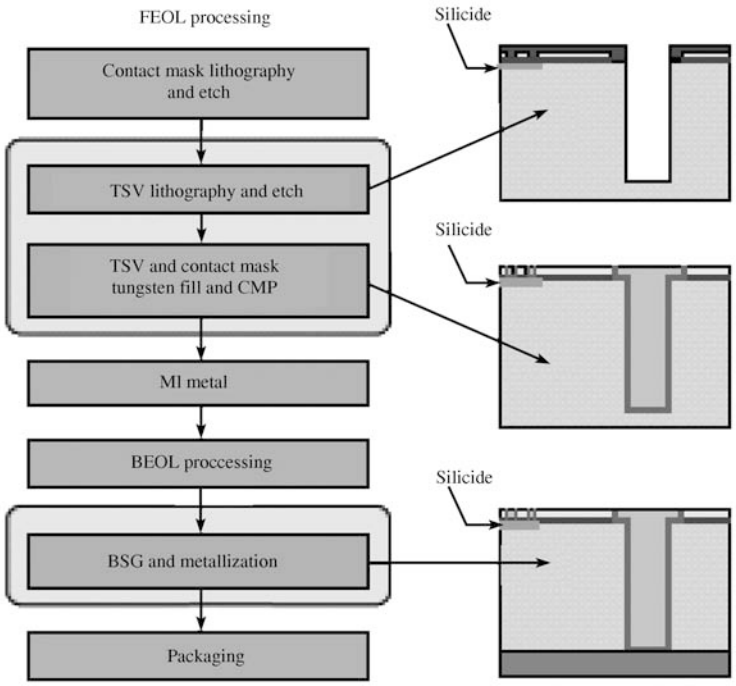

Figure 8 Via middle process flow [25].

additional materials, e.g. polymers, followed by appropriate thermal processing and removal of excess material from the surface. Extensive work has been done in the development of each of these processes, and the characterization of the resulting TSV's at a variety of dimensions and pitches [24–43].

The TSV etch process is directly influenced by the combination of layers and materials through which etching must occur. In a true via-first process, vias are etched at the very beginning, whereas in the instance of via etching after most silicon fabrication is complete, vias are etched last. A comparison of these process flows is shown in Figure 7 [24], whereas a via-middle process flow is shown in Figure 8 [25]. The TSV diameter, depth and pitch are also key factors in the choice of etch method. Constructing a

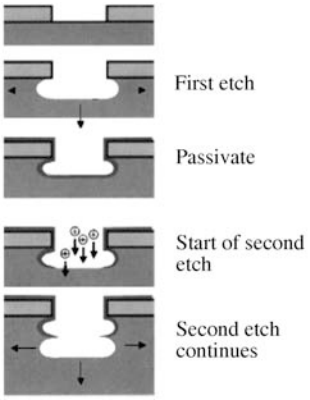

Figure 9 Schematic of the Bosch process [43].

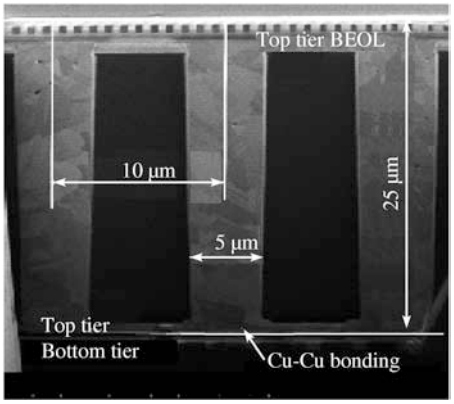

Figure 10 SEM image of TSV's on a 25 μm pitch [42].

25 μm deep TSV with an aspect ratio of ∼5:1 in the middle of the back end process [26] may require a different technique compared to a process that requires very deep TSVs, in the 100 μm range, with aspect ratios approaching 50:1, at the start of silicon processing [25].

For etching through silicon, a commonly employed technique is the Bosch process which has alternating cycles of passivation (C4F8) to prevent lateral etching, followed by Si etch (SF6) [43, 44]. Figure 9 has a schematic of the Bosch process [43]. Ionic bombardment during these cycles removes polymer at the bottom to allow vertical etch. Aspect ratios of better than 40:1 are achievable by this method. Several researchers have used the Bosch method for their TSV evaluations [25, 27, 28, 34, 42]. Others have investigated non-Bosch TSV etch processes, such as a magnetically-enhanced capacitively-coupled plasma etch method, to achieve aspect ratios approaching 30:1 [30] or an enhanced etch process to achieve deep vias with minimal sidewall roughness, i.e. scalloping [32]. Figure 10 shows an SEM image of a 5 μm diameter TSV on a 10 μm pitch, with a depth of 25 μm [42].

While the majority of researchers appear to be using a circular TSV, other form factors for the TSV have also been studied, such as bar vias and annular vias [24, 25, 36]. The form factor of the TSV must be chosen with care since it may influence the subsequent processes, i.e. insulation and metallization. TSV etching may also involve etching various stacks of BEOL (back end of line) dielectrics, if TSV's are introduced mid-stream. Standard RIE (reactive ion etching) techniques may be employed for the BEOL etch portion, followed by a Bosch or other process for the silicon etch portion.

TSV insulation is often a critical step that must ensure electrical isolation of the TSV from the surrounding silicon and other materials. For a via-first process, a thermally grown oxide may fit the bill because of its high quality, and its non-dependence on aspect ratio issues. For via-mid or via-last situations, the typical choice is a deposited oxide that can coat the TSV conformally, such as a PECVD (plasma enhanced chemical vapor deposition) method using TEOS (tetra ethyl ortho silicate) as the primary pre-cursor [28]. Deposition temperatures may range from 100°C to 450°C. Dukovic et al. [32] report the use of an SACVD (subatmospheric chemical vapor deposition) which has high conformality; they indicate that the use of SACVD films is suited to via-first and via-middle flows, whereas a via-last process may need PECVD films due to temperature constraints.

The quality of the oxide may be studied using MIS (metal insulator semiconductor) structures on blanket films. Buchanan et al. [28] have reported a strong dependence of leakage current on the deposition temperature. Further, they have observed that lower temperature depositions yield films whose leakage current drifts with time, which is clearly an undesirable situation. Breakdown voltage, leakage currents at a given field strength, and dielectric constant are all important electrical characteristics of an insulator film. However, material properties such as water absorption and intrinsic film stress are equally important, especially because the former is known to affect electrical properties. Archard et al. [39] have done a detailed analysis of PECVD films, including adequacy of coverage, electrical data, and suppression of OH (hydroxyl group) content.

TSV metal fill, the next step in the process, depends on the form factor of the TSV. The most commonly used form is the cylindrical shape, and the most popular metallization is copper, for its compatibility

with the BEOL process, its high conductivity, and its relative ease of processing. Andry et al. [24] have described an annular via process as well. For a successful copper plating process, it is essential that the prior depositions of diffusion barrier/liner and seed completely cover the TSV surface. Any missing seed, for instance, could lead to plating issues. Detailed studies of copper plating problems, and ways to overcome them can be found in several recent publications [29, 33–35, 37]. Further, annealing studies on the copper TSV have been conducted, and results reported in [42]. Other researchers have focused on Ni alloys as the material of choice [38, 40]. Joseph et al. [25] report on the use of tungsten-filled, multifinger, bar-shaped TSVs in an interposer designed to deliver a low-inductance ground to the package. Each choice of metal/alloy comes with its own set of issues. Copper has a high CTE (coefficient of thermal expansion) mismatch with silicon, leading to real concerns about stress induced by the TSV in the surrounding silicon matrix during thermal excursions. For this reason, some researchers have proposed only a partial filling with copper, followed by a complete filling with a polymer of appropriate physical characteristics [41]. Volant et al. [45] have proposed an annular co-axial TSV that contains a suitable polyimide, to over the thermo-mechanical reliability problem.

2.6 TSV testing

Several studies have been conducted on TSV chain yields and reliability. In one instance, circular copper TSV's of 5 μm diameter and 10 μm depth were built at a ∼9 μm pitch; chains were constructed using wafer to wafer bonding and the cumulative resistance was then measured [46]. The results showed good correlation with calculated values based on the geometry, with negligible contribution from bond interface resistance. The same study also compared tapered vias to straight vias, and concluded that tapered vias were superior in terms of seed coverage and via filling [46].

For silicon carrier applications, test sites were constructed using tungsten vias in either a bar format or an annular via format [24]. The TSV resistances in this exercise were measured to be on the order of 10–20 mΩ with yields on the order of 99.99% at the wafer level. The process used was a via-first process in which TSV's are etched, and lined with insulator in the early part of the process sequence. The metallization can occur either right after that, or it can occur at a much later point. In the latter case, a dummy fill process is needed for the TSV's. Completed TSV chain structures were subjected to thermal cycling, and tested both before and after cycling; the fall out was well below 0.1%, indicating a high level of integrity in the tungsten TSV structures tested.

2.7 TSV impact on devices

Although TSV's are a required feature of 3D integration, their presence has the potential to have ill-effects on device performance. This arises due to the CTE mismatch between metals such as copper, and the surrounding silicon, which leads to create localized stresses in the silicon. The justifiable concern then, is that these stresses could adversely affect device performance. Some investigators have studied this effect, and reported their findings [26, 46–50].

Okoro et al. [46] studied the stress pattern at the TSV edges and in proximal locations of TSV's, using micro Raman Spectroscopy. Cu TSV's of 5 μm diameter were built at a 10 μm pitch; samples were then annealed at 250°C for 30 s, and at 420°C for 20 min. They found that far from the TSV, the shift in the Raman peak (as compared to a control stress-free sample) is zero, indicating no stress. Close to the edge, it became negative, indicating tensile stress. They concluded that when 5 μm TSV's are closer to each other than about 10 μm, their stress fields overlap, and enhance each other. They then determined that any device that is within this range could suffer the consequences of that magnified stress field [46].

Katti et al. [26] built a 3D stacked IC (integrated circuit) using a TSV via-first approach, and also used copper TSV's of 5 μm diameter on a 10 μm pitch. The TSV's were made during the silicon fabrication process, using a 130 nm technology node test site. A two-level BEOL was constructed and the wafer was subsequently attached to a temporary carrier, and thinned. Finally, copper thermo-compression bonds were used to achieve joining at the die level. Integrity testing was then conducted on actual hardware to assess the effect of the 3D processes on n- and p-type devices; the conclusion was that their fabrication methods did not impact their devices negatively [26].

However, Mercha et al. [47] reported the impact of TSV stress on high precision analog devices using a high resolution DAC (digital analog conversion) circuit. TSV's were placed at various distances from MOS (metal oxide semiconductor) devices ranging from 1.7 to 20.7 μm, to determine the transistor 'keep-out' zones [47]. The results show that the TSV's do influence the performance of the devices for particular orientations, and proximity of 2 μm or less. For the nMOSFET device, a shift of −0.5% in ion was observed, compared to the control, while for the pMOSFET device, this was 4.5% compared to the control. When the TSV's are placed at a distance of 20.7 μm, the effect on devices was found to be negligible.

Yang et al. [49] evaluated 130 nm MOSFET's (metal oxide semiconductor field effect transistor) at varying distances from TSV's. Their results show that even at a distance of only 1.1 μm, the MOSFET's show no effect of the TSV's on performance. They further cycled the structures between −55°C and +125°C for 1000 cycles, and still found that there was no degradation in the devices due to TSV proximity. They were, therefore, able to conclude that TSV's did not affect their 130 nm CMOS technology [49].

Okoro et al. [50] studied the induced stresses in silicon caused by copper thermo-compression bonding; they concluded that the extent of the stress distribution around the copper TSV depends strongly on the TSV diameter, and that PMOS devices are more sensitive to stresses induced by the copper TSV than are NMOS devices. The above analyses indicate that keep out zones for devices varies as a function of TSV size and pitch, as well as device sensitivity to stress fields in its vicinity.

2.8 Micro bump technology

One of the key attributes of die to die stacking is a reliable and robust interconnection between the two dies. This has been studied previously using Controlled Collapse Chip Connection (C4) between one thinned die and one full thickness die by Dang et al. [21]. With adequate warpage control of the thinned die, and optimization of handling and release methods on wafers, assembly yield of 100% was demonstrated on die containing several thousands of TSV's. Further, the above demonstration was done using micro C4's of 25 μm diameter at a pitch of 50 μm, and using Pb-free solder alloys in the SnCu (Tin Copper) family. Reliability stressing was also carried out on the two-die stack assembly mounted on a ceramic substrate, with positive results after 1000 deep thermal cycles (DTC's) between −55° and +165°.

Ohara et al. [51] investigated a combined bump technology, wherein copper is electroplated and tin is evaporated, to achieve 5 μm square bumps on a 10 μm pitch, with a very tight distribution of bump height. Micro-joining characteristics and resistances were then evaluated. The study showed good I-V characteristics, and excellent resistance values, compared to pure electroplated CuSn bumps. Characterization of micro-bumps for silicon carrier applications was carried out by Wright et al. [52], who concluded that contact resistance was found to be about the same for eutectic SnPb as well as SnCu solder compositions, and at most 2–3 times larger than the standard 100 μm bumps. Further work in this field has been conducted by others [53–55]. Thus, although microbumps are not mandated for all 3D die stacking, their importance will increase in proportion to the requirement of having a tightly packed grid of interconnections between opposing die.

2.9 Thermo-mechanical integrity & reliability

Beyond the issues of structural integrity during the fabrication process, there is also an overarching concern about the thermo-mechanical reliability of 3D chips. This too stems from the fundamental mismatch of CTE's between TSV metallization such as copper, and the surrounding silicon envelope. Several researchers have studied various aspects of this problem [56–63]. A few of these findings are discussed here.

Modeling using FEM (finite element modeling) has been conducted to enable technologists to get early insights [56]. Complexity in the building of the model arises due to the presence of organic carriers, thermal interface materials, and chip underfill materials, which inherently do not lend themselves to a simple linear elastic problem. Additionally, the pulsing of hotspots during random workloads must

be considered, which further complicates the problem [56]. The thermal characteristics of 3D stacks can actually exacerbate reliability concerns, which is why thermal management of 3D structures is an important field of study [57].

Chen et al. [58] used FEM to investigate first the thermo-mechanical response of Cu/Sn/Ag (copper tin silver) micro-solder joints under accelerated temperature cycling. They subsequently ran a DoE (design of experiment) to evaluate several parameters such as TSV diameter, standoff height of the micro-joint, stiffness of the underfill, etc. [58]. They were able to determine the key factors that influence micro-solder joint reliability; they also concluded that the TSV diameter is the most important control factor in determining the durability of the TSV and the TSV-insulator interface [58].

Amagai et al. [59] used piezo stress sensors to measure local stress in chips with varying degrees of copper TSV density. They found that measured stress increased with copper density; they also performed FEM analysis to predict silicon stresses near TSV's of varying diameter and pitches; they found good agreement between their model and their measurement. Further, the FEM showed that TSV diameter has a more dominant effect on silicon stress than TSV pitch, which is in agreement with Chen et al. [58]. They also found that when TSV annealing temperatures go from 150°C to 400°C, the effective stress at a given distance (4 μm) from the TSV, increases from about 50 MPa compressive to about 100 MPa tensile [59].

Lu et al. [60] also conducted FEM analysis, and concluded that reducing the TSV diameter has a strong influence on lowering the crack driving force that could lead to delamination of the TSV from its insulator. They also studied four different TSV fill materials, and found that tungsten yielded the smallest crack driving force due to the lowest CTE mismatch with silicon, which is completely in line with expectations. They also concluded that two possible mitigation techniques for delaminations are: annular TSVs, and an overlying metal cap on the TSV [60].

3 3D constraints

We spoke earlier about certain constraints that need special consideration. These constraints can be classified in four broad categories: the overhead and design constraints of through silicon vias (TSVs); power delivery and distribution in multiple strata; heat dissipation across the 3D stack; and finally reparability of the 3D stack. In what follows we discuss some applications that circumvent these constraints.

4 Applications

4.1 Image sensors

Today, 3D integration is used extensively in image sensors and several high end phones already employ image sensors that are 3D. An example of such image sensors can be found in Suntharalingam et al. [64].

The key idea in such applications to separate the processing functions from the sensor function so as to maximize the surface area of the optical sensor. This allows for greater signal to noise ratio and resolution.

4.2 Memory stacking

Memory stacking avoids some of the challenges outlined above: memory power is relatively low and makes relatively low demands both on power delivery and heat dissipation. Today, memory (both DRAMs and Flash) is stacked. However, this is mainly done for form factor reasons and often using conventional packaging methods (e.g. Quad Die Package). Each memory die operates fairly independently. As pipelined memory speeds increase, the I/O power of these stacked die increases and today, DRAMs boast some of the most sophisticated I/O serialized links. This however comes at the price of increased circuit complexity and worse power. Today I/O power dominates the total DRAM power for high performance systems and at the overall system level, memory power can account for as much as a third of the total system power. With increased virtualization, the memory requirements are expected to increase even

further with concomitant and unacceptable increases in total power. 3D integration of memory has been proposed as a method to address this problem. In this embodiment that has been demonstrated [1], a master-slave scheme was proposed. Many of the higher circuit elements are activated only on the master die and turned off on the slave die. The authors claim up to a 50% reduction in power which is very significant. We believe that this is an ideal first application of 3D integration and leverages both the use of third dimension to increase volumetric transistor density and the shorter vertical path length means a negligible wiring load that eliminates several copies of the onchip PLLs and I/O drivers.

In principle, these benefits can be realized without 3D through conventional scaling. This allows one to pack twice the bits on the same die area and realize power benefits. The real question is whether which provides a more economic and reliable solution. As DRAMs scale into the sub 45 nm lithography node, and immersion lithography is needed, we expect the equation to favor 3D solutions using previous generation technologies, at least during the initial introduction phase and then move to planar solutions as yield and costs are driven down. Certainly the ability to quadruple (or even more) the number bits using 3D is something that simple scaling cannot compete with. In addition this solution will need to compete with other buffered memory solutions, but there again these solutions increase bit count and performance but at the expense of total chip count (including an ASIC chip) and increased power.

4.3 Embedded memory

Embedded memory in multicore processors is another tailor-made opportunity for 3D integration. Typically today the L3 caches dominate the real estate use in multi-core die. Consider an L3 cache system: this would consist of anywhere between 4 to 16 MB of cache per core depending on workloads being designed for. The bandwidths, latencies and random cycle times required for these applications are quite aggressive. For larger caches, time-of-flight considerations in conventional 2D implementations dominate and a 3D implementation would cut these time-of-flight latencies considerably. Implementing a 3D cache is however not a simple matter. The processor cores require and dissipate considerable power and there are two options for the 3D stacking. The processor on top proximate to the heatsink with the memory die proximate to the laminate. This approach allows the processor to be heat-sunk in a conventional manner. But the power to the processor chip will need to be delivered through the memory chip using TSVs. The power will need to be delivered fairly uniformly and this will disrupt the layout of the memory arrays considerably. In the worst case, the TSVs can detract from the memory efficiency by up to 50% which is not acceptable. Some of this can be mitigated with help of low impedance power redistribution layers but we expect a 10% inefficiency even in the most optimistic case.

An alternative approach is to place the memory die on top proximate to the heat sink. The memory die requires significantly (0.1X) less power and can be supplied with a minimal number of TSVs and this no disruption of the memory chip efficiency. The TSVs through the processor chip can be placed judiciously without material impact to the processor chip layout. The drawback of this scheme lies in the fact that there will be a small but noticeable increase in the processor temperature and peak temperature. This will manifest itself in a small degrade in processor performance, though in the case of Hi K implementations, this may be acceptably low.

5 Concluding remarks

Despite the issues associated with the use of TSV's in silicon and other semiconductor materials, the need for 3D stacking is unquestioned. Many publications over the last several years have indicated that companies are either already manufacturing 3D chips or have plans to do so in the near future [65–78]. Ultimately, the success of any manufacturable 3D integration solution rides on several factors: 1) the choice of TSV technology, which in turn is determined by its compatibility with the rest of the fabrication process, including the bonding stage and method, and the requirements that are placed upon it from a systems perspective; 2) the robustness and thermo-mechanical reliability of the fully integrated structure; and 3) cost/yield considerations. In general, die to die bonding may be regarded as an important first

foray into 3D integration. However, to achieve true circuit level 3D integration, there is no choice but to achieve bonding at the silicon, i.e. wafer level, where the CPU has rapid access to memory, without the burden of inductance and the longer paths associated with solder joints.

References

1 Morgan T P. IBM's zEnterprise 196 CPU: Cache is king-the fastest CPU in the world. http://www.theregister.co.uk/2010/07/23/ibm_z196_mainframe_processor/

2 Zeng A, Lu J, Rose K, et al. First order performance prediction of cache memory with wafer-level 3D integration. IEEE Des Test Comput, 2005, 22: 548–555

3 Black B, Annavaram M, Brekelbaum N, et al. Die stacking (3D) microarchitecture. In: The 39th Annual IEEE/ACM Int'l Symposium on Microarchitecture, 2006. 469–479

4 Peltola T, Mansikkamaki P, Ristolainen E O. 3D integration of electronics and mechanics. In: Proc. of the Int'l Symposium on Advanced Packaging Materials, 2005. 5–8

5 Charlet B, Cioccio D, LeDuc P. Enabling technologies for 3D system on chip (SOC) integration and examples of 3D integrated structures. In: Proc. of the IEEE Int'l Conference on Integrated Circuit Design and Technology, 2007. 1

6 Yole Development, Market Report, Nov 2007

7 Bougard B, Marchal P, Benini L, et al. Hot topic-3D integration or how to scale in the 21st century. In: Design, Automation and Test, 2008. 1516

8 Sadaka M, Radu I, DiCioccio L. 3D integration-advantages, enabling technologies & applications. In: Proc. of the IEEE Int'l Conference on IC Design and Technology, 2010. 106–109

9 Choudhury D. 3D integration technologies for emerging Microsystems. In: Proceedings of the IMS, 2010

10 Koester S, Young A M, Yu R R, et al. Wafer-level 3D integration technology. Special Issue of IBM J Res Dev, 2008, 52: 583–597

11 Ohba T. 3D large scale integration technology using wafer on wafer (WOW) stacking. In: Proc of the IEEE Int'l Interconnect Technology Conference, 2009

12 Topol A W, LaTulipe D C, Shi L, et al. Enabling SOI-based assembly technology for 3D integrated circuits (ICs). In: Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, 2005. 352–355

13 Iyer S S, Auberton-Herve A J. Silicon wafer bonding technoloy for VLSI and MEMS applications. In: EMIS Processing Series 1, INSPEC, 2002

14 Ziptronix, Inc. ZiBond direct wafer bonding technology. see http://www.ziptronix.com/techo/zibond.html

15 University of Texas at Arlington, Automation and Robotics Research Institute, http://arri.uta.edu/micromanufacturing/micropackaging/3D_packaging.html

16 Williams G, O'Hara P, Moore J, et al. A review of wafer bonding materials and characterizations to enable wafer thinning, backside processing, and laser dicing. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2009

17 Huyghebaert C, Van Olmen J, Civale Y, et al. Cu to Cu interconnect using 3D TSV and wafer to wafer thermo-compression bonding. In: Proc. of the IEEE Int'l Interconnect Technology Conference, 2010. 1–3

18 Webb R. Temporary bonding enables new processes requiring ultra-thin wafers. In: Solid State Technology, www.solid-state.com, February 2010

19 Bieck F, Spiller S, Molina F, et al. Carrierles design for handling and processing of ultrathin wafers. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 316–322

20 Sakuma K, Andry P S, Tsang C K, et al. 3D chip-stacking technology with TSV's and low-volume lead-free interconnections. Special Issue of IBM J Res Dev, 2008, 52: 611–621

21 Dang B, Wright S L, Andry P S, et al. 3D chip stacking with C4 technology. Special Issue of IBM J Res Dev, 2008, 52: 599–609

22 Van Olmen J, Coenen J, Dehaene W, et al. 3D stacked IC demonstrator using hybrid collective die-to-wafer bonding with copper TSV. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2009

23 Leduc P, Assous M, DiCioccio L, et al. First integration of Cu TSV using die-to-wafer direct bonding and planarization. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2009

24 Andry P S, Tsang C K, Webb B C, et al. Fabrication and characterization of robust TSVs for silicon-carrier applications. Special Issue of IBM J Res Dev, 2008, 52: 571–581

25 Joseph A J, Gillis J D, Doherty M, et al. TSV's enable next-generation SiGe power amplifiers for wireless communications. Special Issue of IBM J Res Dev, 2008, 52: 635–648

26 Katti G, Mercha A, Van Olmen J, et al. 3D stacked ICs using Cu TSVs and die to wafer collective bonding. In: Proc. of the IEEE Int'l Electron Devices Meeting, 2009. 1–4

27 Alapati R, Travaly Y, Van Olemn J, et al. TSV metrology and inspection challenges. In: IEEE 3D System Integration

Conference, 2009
28 Buchanan K, Burgess S, Giles K, et al. Etch, dielectrics and metal barrier-seed for low temperature TSV processing. In: IEEE 3D System Integration Conference, 2009
29 Yoon S W, Yang D W, Koo J H, et al. 3D TSV processes and its assembly/packaging technology. In: IEEE 3D System Integration Conference, 2009
30 Teh W H, Caramto R, Arkalgud S, et al. Magnetically-enhanced capacitively-coupled plasma etching for 300 mm wafer-scale fabrication of Cu TSV's for 3D logic integration. In: Proc. of the IEEE Int'l Interconnect Technology Conference, 2009. 53–55
31 Kaiho Y, Ohara Y, Takeshita H, et al. 3D integration technology for 3D stacked retinal chip. In: IEEE 3D System Integration Conference, 2009
32 Dukovic J, Ramaswami S, Pamarthy S, et al. TSV technology for 3D integration. In: IEEE Memory Workshop, 2010. 1–2
33 Li H Y, Liao E, Pang X F, et al. Fast electroplating TSV process development for the via-last approach. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 777–780
34 Chua T T, Ho S W, Li H Y, et al. 3D interconnection process development and integration with low stress TSV. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 798–802
35 LimB O, Choi K S, Eom Y S, et al. Optimized TSV process using bottoms-up electroplating without wafer cracks. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1642–1646
36 Xie B, Shi X Q, Chung C H, et al. Novel sequential electro-chemical and thermo-mechanical simulation methodology for annular TSV design. 3D TSV processes and its assembly/Packaging technology. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1166–1172
37 Malta D, Gregory C, Temple D, et al. Integrated process for defect-free copper plating and chemical-mechanical polishing of TSV's for 3D development. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1769–1775
38 Inoue F, Yokoyama T, Miyake H, et al. Conformal deposition of electroless barrier and seed layers. In: Proc. of the IEEE Int'l Interconnect Technology Conference, 2010. 1–2
39 Archard D, Giles K, Price A, et al. Low temperature PECVD of dielectric films for TSV applications. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 764–768
40 Kawano M, Takahashi N, Komuro M, et al. Low-cost TSV process using electroless Ni plating for 3D stacked DRAM. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1094–1099
41 Bouchoucha M, Chausse P, Henry D, et al. Process solutions and polymer materials for 3D-WLP TSV filling. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1696–1698
42 Huyghebaert C, Van Olmen J, Chukwadi O, et al. Enabling 10 μm pitch hybrid Cu-Cu IC stacking with TSVs. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1083–1087
43 Craigie C J D, Sheehan T, Johnson V N, et al. Polymer thickness effects on Bosch etch profiles. Vac Sci Technol B, 2002, 20: 2229–2232
44 Kok K W, Yoo W J, Sooriakumar K, et al. Investigation of in situ trench etching process and Bosch process for fabricating high-aspect-ration beams for micromechanical systems. J Vac Sci Tech B: Microelectron Nanometer Structures, 2002, 20: 1878–1883
45 Volant R, Farooq M G. Coaxial TSV for 3D applications with polyimide dielectric. In: Symposium on Polymers for Microelectronics Conference, 2010
46 Okoro C, Yang Y, Vandevelde B, et al. Extraction of the appropriate material property for realistic modeling of TSVs using μ-Raman spectroscopy. In: Proc. of the IEEE Int'l Interconnect Technology Conference, 2008. 16–18
47 Mercha A, Redolfi A, Stucchi M, et al. Impact of thinning and TSV proximity on high-k/metal gate first CMOS performance. In: Proc. of the IEEE VLSI Technology Conference, 2010. 109–110
48 Khan N, Alam S M, Hassoun S. TSV-induced noise characterization and noise mitigation using coaxial TSVs. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2009
49 Yang Y, Katti G, Labie R, et al. Electrical evaluation of 130-nm MOSFETs with TSV proximity in 3D-SIC structure. In: Proc. of the IEEE Int'l Interconnect Technology Conference, 2010. 1–3
50 Okoro C, Gonzales M, Vandevelde B, et al. Prediction of the influence of induced stresses in silicon on CMOS Performance in a Cu-through-via interconnect technolog. In: Proc. of the IEEE Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, 2007. 1–7
51 Ohara Y, Noriki A, Sakuma K, et al. 10 m fine pitch Cu/Sn micro-bumps for 3-D super-chip Stack. In: IEEE 3D System Integration Conference, 2009
52 Wright S L, Polastre R, Gan H, et al. Characterization of micro-bump C4 interconnects for Si-carrier SOP applications. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2009. 633–640
53 Yoon S W, Ku J H, Suthiwongsunthorn N, et al. Fabrication and packaging of microbump interconnections for 3D TSV. In: IEEE 3D System Integration Conference, 2009

54 Horibe A, Yamada F. Advanced 3D chip stack process for thin dies with fine pitch bumps using pre-applied inter chip fill. In: IEEE 3D System Conference, 2009
55 Agarwal R, Zheng W, Limaye P, et al. Cu/Sn microbumps interconnect for 3D TSV chip stacking. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2010. 858–863
56 Sri-Jayantha S M, McVicker G, Bernstein K, et al. Thermomechanical modeling of 3D electronic packages. Special Issue of IBM J Res Dev, 2008, 52: 623–634
57 Emma P G, Kursun E. Is 3D chip technology the next growth engine for performance improvement? Special Issue of IBM J Res Dev, 2008, 52: 541–552
58 Chen A, Song B, Wang X, et al. Thermo-mechanical reliability analysis of 3D stacked-die packaging with TSV. In: IEEE 11th Int'l Conference on Electronic Packaging Technology & High Density Packaging, 2010. 102–107
59 Amagai M, Suzuki Y. TSV stress and modeling. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1273–1280
60 Lu K H, Ryu S K, Zhao Q, et al. Thermal stress induced delamination of TSVs in 3D interconnects. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 40–45
61 Sunohara M, Sakaguchi H, Takano A, et al. Studies on electrical performance and thermal stress of a silicon interposer with TSVs. In: Proceedings of the IEEE Electronic Components and Technology Conference, 2010. 1088–1093
62 Pang X F, Chua T T, Li H Y, et al. Characterization and management of wafer stress for various pattern Densities in 3D integration technology. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 1866–1869
63 Trigg A D, Yu L H, Zhang X, et al. Design and fabrication of a reliability test chip for 3D-TSV. In: Proc. of the IEEE Electronic Components and Technology Conference, 2010. 79–83
64 Suntharalingam V, Rathman D, Prigozhin G, et al. Back-illuminated three-dimensionally integrated CMOS image sensors for scientific applications. In: Proc of SPIE Vol. 6690, 2007. 669009-1–669009-9
65 Gupta S, Hilbert M, Hong S, et al. Techniques for producing 3D ICs with high-density interconnect. In: VLSI Multi-Level Interconnection Conference, 2004
66 Patti R. Lessons learned in the quest for 3D products. In: IMAPS Global Business Council, March 2009
67 Garrou P. Insights from the leading edge. www.electroiq.com/index/packaging, October 2010
68 Yole Development Market Report. Advanced Packaging: 3D IC and TSV Interconnects 2010
69 Elpida, PTI, and UMC partner on 3D IC integration development for Advanced technologies including 28 nm. www.elpida.com, June 2010
70 Samsung develops 3D memory package that greatly improves performance using less space. www.samsung.com, April 2006
71 Sematech's 3D interconnect program. www.sematech.org, 2010
72 Jiang T, Shijian L. 3D integration—present and future. In: Proc. of the IEEE Electronic Components and Technology Conference, 2008. 373–378
73 IBM work on 3D chip stacking will take Moore's Law to 2025. www.nextbigfuture.com, March 2010
74 Toshiba Eyes 3D memory chips with new factory investment. www.pcworld.com, May 2010
75 Kujala K. Memory stacking to TSV? In: Semicon, Taiwan, 2010
76 Mirkarimi L, Huynh M, Savalia P, et al. 3D interconnects for dense die stack packages. In: IEEE 3D System Integration Conference, 2009
77 Fritzsch T, Mrobko R, Baumgartner T, et al. 3D thin chip integration technology—from technology development to application. In: IEEE 3D System Integration Conference, 2009
78 Kang U, Chung H J, Heo S, et al. 8 Gb 3D DDR3 DRAM using through-silicon-via technology. In: IEEE ISSCC, 2009. 130–131, 131a