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论 文
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超薄 SiO_x 钝化层所导致的半导体-绝缘体-半导体异质结高频隧道电容溢出现象

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摘要 从高频电容电压特性测试中发现的隧道电容溢出现象出发, 研究了具有超薄钝化层的半导体-绝缘体-半导体(semiconductor-insulator-semiconductor SIS)异质结器件界面处独特的电荷存储特性. 从SIS 1 MHz频率下的*CV*特性可知, 当外加偏压小于V_T(voltage tunneling)时, SIS界面处于耗尽状态, 而当外加栅压超过V_T之后, SIS的高频电容将远超仪器量程趋于无穷大, 可概括称为隧道电容溢出现象. 从SIS的XPS(X-ray photoemission spectroscopy)深度剖析结果可知, 具有不同厚度的ITO(indium tin oxide)的SIS器件界面钝化层所含元素组分并无差别. 但从TEM(transparent electron microscope)的结果来看, 钝化层厚度随ITO的增加而增加, 分析表明不同ITO厚度的SIS所对应V_T值不同的主要原因是由于钝化层厚度的不同. 通过对实验结果的分析, 本文给出了隧道电容溢出现象的载流子输运的能带模型. 结果表明, 隧道电容溢出是由于超薄钝化层无法使大量电子在界面处积累所致. 且同一器件隧道电容溢出现象是可重复的, 不会对器件带来物理损伤, 这是采用直接磁控溅射工艺制备SIS异质结太阳电池稳定性的体现.

关键词 超薄钝化层, 隧道 *CV*, 半导体-绝缘体-半导体, 异质结, 太阳电池

SIS(semiconductor-insulator-semiconductor)结构异质结源自于MOS(metal-oxide-semiconductor)结构, 具有成本较低、结构简单、性能稳定和理论效率高等优点, 因此对MOS和SIS的研究一直都是太阳电池和集成电路应用方面的热点[1~5]. SIS结构一般由TCO层、界面绝缘层和Si基底3部分组成, 其中, 当界面绝缘层厚度降低至1~5 nm时, 界面处载流子可通过隧道效应穿过钝化层[6~8]. 超薄的钝化层具有隧穿接触和钝化界面等多重作用, 其钝化效果反映了界面处缺陷态密度, 而界面态则直接影响载流子的输运和收集, 从而影响电池光伏特性[9~12].

电容是表征一个器件存储电荷的能力, 在对界面处的缺陷态进行定量测量表征时, 无论是高低频法还是深能级瞬态谱(deep-level transient spectroscopy, DLTS), 均需要借助于*CV*(capacitance-voltage)特性来探测界面处的电荷分布情况[13,14]. 在采用安捷伦*CV*系统测量SIS的高频电容电压特性时发现, 当外加电压超过某一特定数值V_T(voltage tunneling)后, 微分电容值出现远远超过量程, 趋于无穷大的现象, 可简称这种现象为隧道电容溢出现象. 由于在前人的研究内容中并未见到对此现象的描述与解释, 本文借助于透射电子显微镜(transparent electron microscope, TEM)和X射线光电子谱(X-ray photoemission spectroscopy, XPS)深度剖析以及安捷伦*CV*测试系统, 通过能

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Li Y, Gao M, Wan Y Z, et al. The high-frequency tunnel capacitance overload phenomenon of semiconductor-insulator-semiconductor heterojunction caused by the ultra-thin interfacial layers (in Chinese). Chin Sci Bull, 2017, 62: 3385–3391, doi: 10.1360/N972016-00582

带模型给出了隧道电容溢出现象的载流子输运过程.

1 器件制备与表征

SIS异质结器件的制备大致可分为3步. 首先选取太阳能级n型直拉单晶硅作为衬底, 晶向为(100), 厚度为(150±3) μm, 电阻率为1.5~3.0 Ω cm, 样品尺寸1.0 cm×1.0 cm, 采用RCA标准清洗法对硅片表面进行清洗[4]; 接着利用JGP-450C型磁控溅射仪, 在40 sccm流动氩气、室温、1 Pa的环境下, 以100 W的射频溅射功率制备得到ITO (indium tin oxide)厚度分别为80, 150和250 nm的SIS异质结器件; 最后在4×10^{-3} Pa的气压下, 用DM-450C型真空蒸发设备在SIS前表面镀上约10 μm厚Ag/Al栅电极, 在背表面镀上Al电极. 实验中所采用的陶瓷靶材由90 wt%的In_2O_3和10 wt%的SnO_2高温烧结而成, 磁控溅射所得ITO薄膜载流子浓度为4×10^{20}~5×10^{20} cm^{-3}, 迁移率为30~40 $cm^2/(V\ s)$, 电阻率为2×10^{-4}~5×10^{-4} Ω cm.

为探究隧道电容溢出现象发生的根本原因和载流子输运的物理过程, 本文采用了JEM-2010F型TEM、ESCALAB-250Xi型XPS、HL5500-PC型HALL效应测试仪、Keysight公司生产的E4980A型*CV*(电容电压)测试系统与Keithly2400型太阳光模拟器对SIS器件进行表征, 分别对钝化层的厚度、钝化层处元素组分、各层的导电特性和器件的光伏特性以及*CV*特性进行了测量分析.

2 分析与讨论

2.1 SIS隧道电容溢出现象

由于SIS器件与MOS器件在结构上的类似, 接下来先简要介绍MOS结构在高频条件下的*CV*特性, 再详述SIS的隧道电容溢出现象. 理论上推导理想MOS模型的*CV*特性包含3个前提条件, 分别为金属半导体功函数差为零、绝缘层内无电荷且完全不导电以及绝缘层与半导体界面处不存在任何界面态[15]. 基于这3个理想条件, 以n-Si为例, 可将MOS结构电容电压特性分为4个区段: (1) 反型区, 如图1(a)所示, 当栅极上所加负偏压较大时, 硅表面的本征费米能级E_i在靠近绝缘层的表面处高于费米能级E_F, 使大量空穴进入价带顶E_V并在硅表面处累积, 形成空穴反型层; (2) 耗尽区, 如图1(b)所示, 硅表面处的电子耗尽, 有耗尽区形成, 此时耗尽区宽度随着栅极偏压变小而变

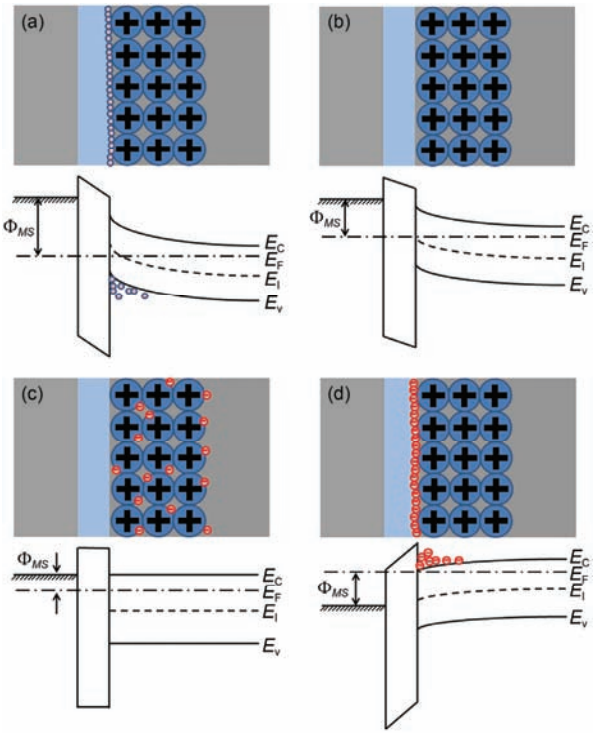

图 1 (网络版彩色)MOS结构空间电荷区载流子分布示意图与对应能带图. (a) 界面反型状态; (b) 界面多子耗尽; (c) 界面处平带状态; (d) 界面多子积累

Figure 1 (Color online) Carriers' distribution in the space charge region of the MOS structure and the corresponding energy band. (a) Inversion state of the interface; (b) majority carriers' depletion of the interface; (c) flat band state of the interface; (d) majority carriers' accumulation of the interface

窄; (3) 平带点, 如图1(c)所示, 栅极电压减小到某个临界值, 恰好使得硅表面的能带与硅体内的能带持平, 此时耗尽区宽度趋于零; (4) 电子积累区, 如图1(d)所示, 栅极正向偏压较大, 硅表面处E_C小于或等于费米能级E_F, 大量电子跃迁到E_C并在硅表面处积累形成电子积累层. 对应于以上4个不同外加栅压的区间, 即可得到图2实线所示MOS结构高频*CV*曲线.

从图2中可以看到界面钝化良好的MOS结构高频(1 MHz) *CV*特性随着栅极偏压的变化可有反型、耗尽和多子积累(此处多子为电子)3个阶段, 电容随偏压变化呈一个倾斜的"S"型[15]. 而具有超薄钝化层的SIS (ITO/SiO_x/n-Si)结构隧道电容溢出现象如图2中虚线所示, 可见其电容无法进入电子积累区, 高频*CV*曲线呈一个"J"型. 对隧道电容溢出现象的反复试探发现, 它具有电容溢出后可恢复、隧道电容溢出电压V_T值相对确定(浮动不超过0.1 V)的特点, 且对应不同SiO_x钝化层厚度值, 隧道电容溢出电压V_T值如

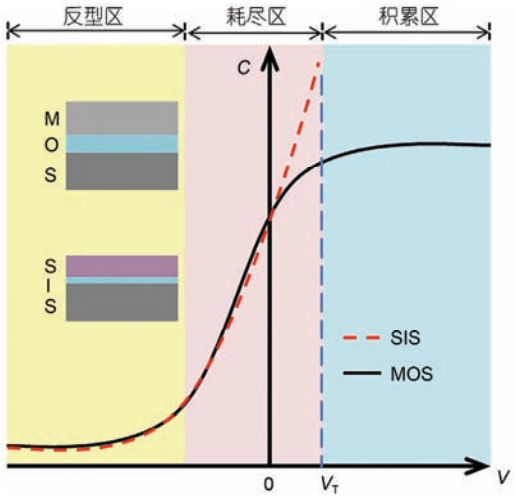

图 2 (网络版彩色)MOS与SIS高频*CV*特性比较(以n-Si为例). 插图为结构对比, 主要差异为钝化层厚度

Figure 2 (Color online) High frequency capacitance voltage of the SIS structure contrast to MOS structure (n-type silicon substrate), the insert is the structure comparison of MOS and SIS, in which the main difference is the thickness of the passivation layer

表1所示.

由前面所描述的SIS制作工艺过程可知, SIS结构与MOS结构在组成部分上, 唯一差别就是前者的ITO取代了MOS结构的金属层. 由ITO的电阻率可知其导电性很好, 又因为ITO厚度在250 nm以下, n-Si约为150 μm, 所以外加偏压绝大部分降在n-Si上, 而硅基上的偏压主要在空间电荷区上. 实验表明ITO与上电极形成了良好的欧姆接触, 因此在本文的分析中, ITO的电阻值以及ITO与上电极的接触电阻忽略不计. SIS与理想的MOS结构最主要的差别在于钝化层的不同, 包括在钝化层的厚度、缺陷浓度和介电常数等, 这也是造成SIS的"J"型*CV*曲线不同于MOS的"S"型*CV*的主要原因, 接下来详细讨论SIS的特性与对隧道电容溢出现象的分析.

2.2 SIS的性能与分析

SIS光伏特性测量结果如图3(a)所示, 可见不同ITO厚度的SIS异质结均展现了良好的光伏转换特性, 且当ITO厚度为150 nm时, 开路电压为0.48 V, 短路电流28.23 mA/cm^2, 填充因子为69.96%, 效率可达9.48%. 开路电压是异质结内建电场的直接反应, 从0.48 V可见SIS异质结内部形成了有效的内建电场. 短路电流是器件能够有效收集载流子的直观度量, 从短路电流28.23 mA/cm^{2}可知, SIS内部的载流子复合并没有给器件整体特性带来灾难性影响, 由此可知异质结界面处的钝化效果良好, 这一点从填充因子FF达到69.96%亦可得到佐证.

图3(b)为实验所得SIS异质结1 MHz的*CV*特性,

表 1 V_T值随SiO_x厚度的变化与拟合内建电场值

Table 1 V_T dependence of the SiO_x thickness and the corresponding matching value of the build-in field

ITO(nm)	SiO_x(nm)	*V*-build-in(V)	*V*-tunnel(V)
80	1.29	0.396	1.40
150	1.43	0.533	1.95
250	1.54	0.539	2.20

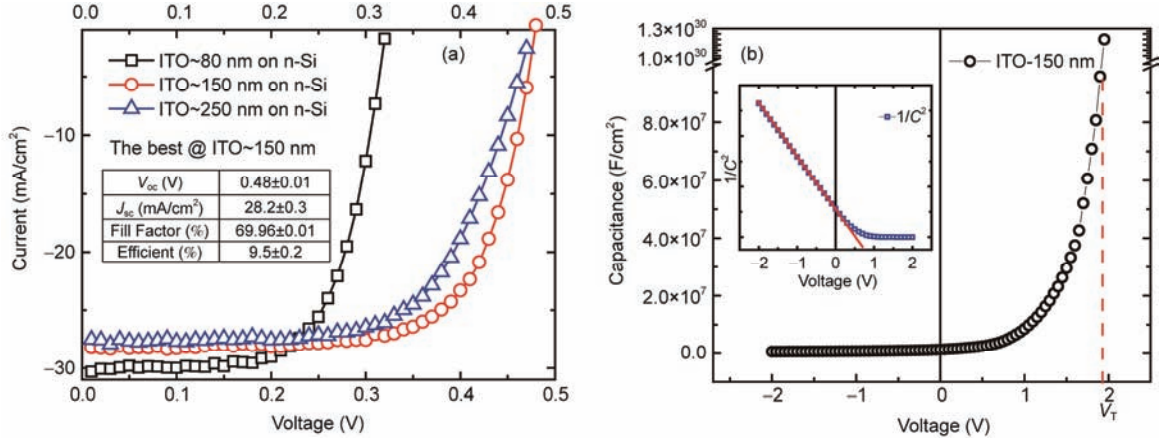

图 3 (网络版彩色)ITO厚度分别为 80, 150 和 250 nm的SIS异质结光照下电流电压特性(a)和ITO厚度为 150 nm的SIS黑暗条件下电容电压特性(b)

Figure 3 (Color online) (a) The photovoltaic conversion characteristics of the SIS heterojunction with ITO thickness of 80, 150 and 250 nm, respectively; (b) the 1 MHz capacitance voltage of the SIS with 150 nm ITO layer under dark condition

参照文献[7]中的计算图，可见实验所得与理论计算结果吻合良好. 通过拟合实验测得的$1/C^2$-V曲线(图3(b)中插图)，可知SIS电容的上升均处在耗尽区，当外加栅压大于V_T时，高频电容远超量程趋于无穷大，即SIS高频电容无法进入多子积累区，出现隧道电容溢出现象. 由图中SIS异质结电容可进入反型区可知，空穴可以在硅表面累积，屏蔽内部电荷从而使反型区的电容保持为一常数，这就可以排除隧道电容溢出是钝化层SiO_x的不均匀性所导致的猜测. 拟合不同ITO厚度的SIS得到内建电场，与测量得到的V_T值，可得表1隧道电容溢出电压V_T与SIS内建电场的对比. 一般来说，内建电场越强，需要的V_T也要更大才能出现隧道电容溢出现象. 考虑到不同ITO厚度的电阻率均在10^{-4} Ω cm的量级，其优良的导电性堪比金属，由此可以肯定电压降在耗尽区和硅基上的数值是远大于在ITO上的，在ITO上的电压降导致的V_T数值的增大可以忽略不计.

在SIS异质结钝化层的材料选择中，干法和湿法热氧化生成的SiO_2钝化效果是较为理想的[16]. 从图3(a)中SIS展示出的优良的光伏转换特性可知其界面钝化效果良好，然而在制作过程中并无特意引入钝化层的独立工艺步骤，由此可知是磁控溅射过程中自然生长的硅氧化合物[1]. 为辨别这层自然生长而成的钝化层的元素组分情况，采用XPS深度剖析功能对SIS(ITO/SiO_x/n-Si)结构界面区进行测量，得到如图4(a)所示各元素相对含量的百分比. 当刻蚀时刻为960 s时，其Si_2p态XPS图谱对应SiO_x/n-Si界面区，分峰结果如图4(b)所示，可知钝化层中含有Si_2O，SiO，Si_2O_3和SiO_2等化合物，即SiO_x($1\leqslant x\leqslant 2$). 对于不同ITO厚度的SIS异质结器件，其钝化层SiO_x($1\leqslant x\leqslant 2$)的化学成分无明显差别[3]，因此其电导率和热稳定性均相同.

ITO厚度分别为80，150和250 nm的SIS结构TEM截面图如图5(a)~(c)所示. 由图可知，其对应的钝化层SiO_x($1\leqslant x\leqslant 2$)主要为非晶态，且厚度依次为1.29，1.43和1.54 nm. 而XPS对不同ITO厚度的SIS结构分析表明，其钝化层SiO_x($1\leqslant x\leqslant 2$)的化合态无明显差别，且文献[17]中的计算表明随着钝化层SiO_x厚度增加，电子隧穿几率降低，再由表1可知，V_T值随着钝化层SiO_x($1\leqslant x\leqslant 2$)厚度增加而递增，故钝化层的厚度是影响隧道电容溢出V_T值的主导因素.

综上所述，当SIS异质结栅极偏压大于或等于V_T时，由于钝化层SiO_x太薄，大量电子隧穿通过钝化层而不能在界面处累积，从而使器件的高频电容趋于无穷大. 这也是为什么隧道电容溢出的电容值趋于无穷大却不会损坏SIS，因为隧穿溢出并没有超出各层的导电极限，不会对各层造成不可逆的物理损伤. 至于ITO厚度不同的SIS器件对应不同的V_T值，是因为随着ITO厚度的增加，钝化层SiO_x厚度也增加. Si-O_x层越厚，电子隧穿的几率越低[18]，为达到相同的隧穿电子数目，界面处需要更多的电子，因此达到隧道电容溢出的电压V_T也就越大. 换言之，SIS的隧道电容溢出现象是由钝化层SiO_x超薄的特殊性所直接导致的.

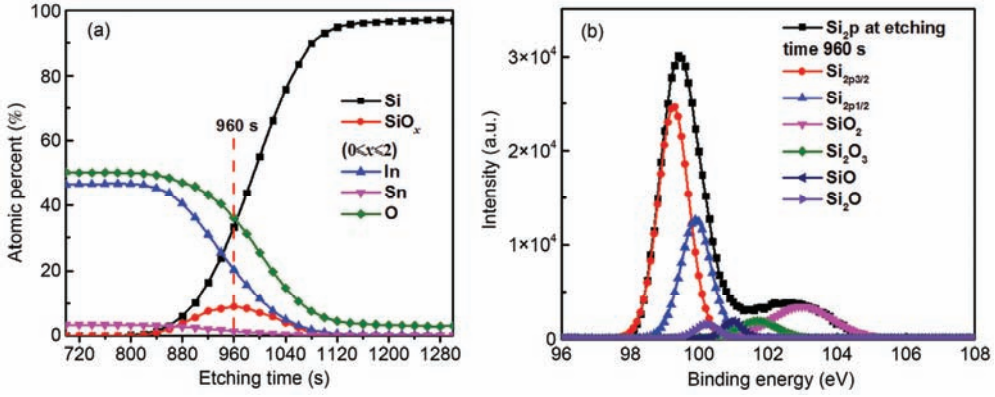

图 4 (网络版彩色)XPS深度剖析测量ITO厚 150 nm的SIS异质结界面处元素组分结果. (a) 深度剖析SIS结构界面处各元素分布; (b) 与刻蚀时刻 960 s对应的Si_2p态

Figure 4 (Color online) XPS depth profiling of the interface within the SIS heterojunction with 150 nm ITO. (a) The elements percentage content of the interface; (b) the Si_2p state corresponding to the etching time at 960 s in (a)

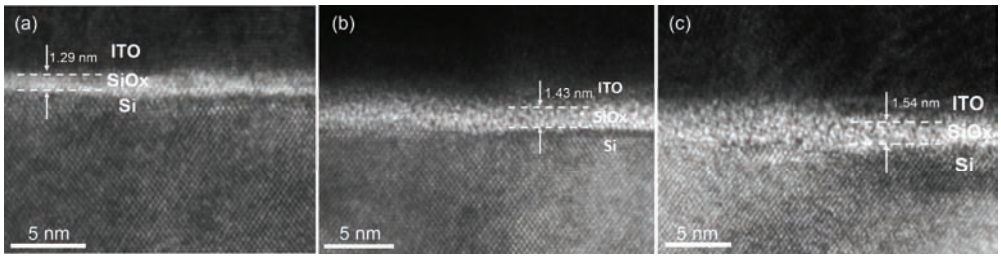

图 5 ITO厚度分别为 80 (a), 150 (b)和 250 nm (c)的SIS结构截面图

Figure 5 The cross profile TEM photograph of the SIS interface, corresponding to the ITO thickness of 80 (a), 150 (b) and 250 nm (c)

2.3 SIS隧道电容溢出现象的载流子输运模型

MOS结构硅表面处于电子积累状态时，能带示意图如图6(a)所示．通过前面的分析可知，在SIS器件隧道电容溢出时，电子从硅表面输运到ITO层的过程如图6(b)所示．随着正向栅极偏压逐渐增大至接近V_T时，硅表面处的E_C向下弯曲，逐渐接近E_F．当偏压大于等于V_T时，界面处E_F将与E_V重合或高于E_V．费米能级E_F代表了半导体中电子的填充水平，费米能级以下可认为是满态．E_V与E_F重合或者低于E_F，将使大量电子进入硅表面的E_C．MOS结构中界面氧化层足够的厚，因此大量的电子可以在硅表面与氧化层的界面处积累，累积的电子可以屏蔽外加偏压对耗尽区宽度的调控作用，所以MOS的电子积累区电容趋于常数．与MOS结构不同，SIS结构的钝化层厚度仅为1~2 nm，当外加偏压大于等于V_T时，电子可以通过隧道效应穿过界面SiO_x层进入ITO中，如图6(b)所示，而不会在硅表面与钝化层界面处累计，从而出现隧道电容溢出现象．又由于SiO_x钝化层的厚度是确定的，即隧穿几率是确定的，当E_V与E_F重合或者低于E_F时，硅表面的电子数目呈指数倍增长，因此隧穿的电子数目将倍增．高频电容探测的是单位电压变化下电荷的变化，此时也将变得极大，远远超出仪器的量程．

电容电压特性是测量器件界面特性最为重要的依据之一，例如在测量器件界面态时，无论是DLTS(深能级瞬态谱)还是准静态法，都是用*CV*来推测其数值[14,19,20]．在对SIS改变频率测量其*CV*时，低频*CV*的电容值会一直正负跳跃而无法探测，在高频时又会出现图3(b)所示结果，即会有隧道电容溢出现象，且不同SiO_x厚度对应不同V_T值．相比于反型状态下，同样一层钝化层空穴却可以累积在界面处，屏蔽外加偏压对电容值的影响，可知高频探测电压下，空穴和电子隧穿的概率并不相等．

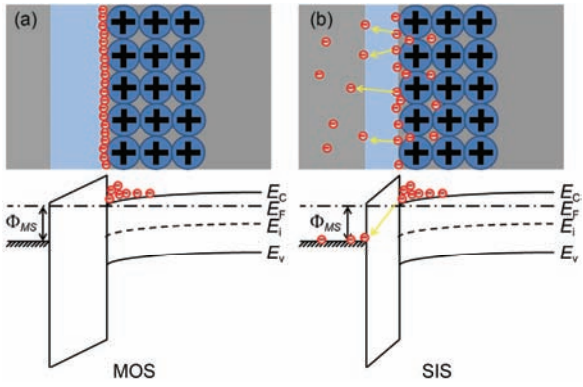

图 6 (网络版彩色)SIS隧道电容溢出过程与MOS多子积累对比示意图. (a) MOS界面处电子积累; (b) SIS界面处电子隧穿

Figure 6 (Color online) The schematic diagram of the high-frequency tunnel capacitance overload phenomenon in the SIS heterojunction contrast to the majority carriers' accumulation (here is the electrons accumulation) in the MOS structure. (a) The electrons accumulated at the MOS interface; (b) the electrons tunnel through the insulator layer of the SIS heterojunction

3 结论

本文从偶然发现的隧道电容溢出现象出发，探究了具有超薄钝化层的SIS异质结特有的隧道电容溢出现象，并用能带模型解释了隧道电容溢出时载流子输运过程．太阳光模拟器测得的*IV*特性表明实验所得SIS异质结具有良好的光伏转换特性，通过安捷伦*CV*测试系统所得SIS电容电压特性，拟合得到了具有不同ITO厚度的SIS内建电场值．XPS深度剖析结果表明，ITO厚度不同的SIS异质结界面处的元素组分与含量一致，但TEM显示钝化层SiO_x的厚度随着ITO厚度的增加而增加，由此可知隧道电容溢出现象是由SIS异质结的超薄钝化层所直接导致．当外加偏压大于V_T时，大量电子进入硅表面的导带底E_C，而与钝化层较厚的MOS不同，电子并不能在SIS界面处积

累，而是直接隧穿通过SiO_x进入ITO，从而导致高频电容趋于无穷大并远超仪器的量程．电容电压特性对于测量各类异质结界面特性至关重要，而高频*CV*在测量界面态中更是不可或缺．隧道电容溢出现象的存在，正是各种基于电容电压特性测量SIS异质结界面态的方法难以奏效的主要原因．但从另一个角度来说，这种可恢复的隧穿电容特性也是SIS异质结作为太阳电池稳定性的体现．

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Summary for “超薄 SiO_x 钝化层所导致的半导体-绝缘体-半导体异质结高频隧道电容溢出现象”

The high-frequency tunnel capacitance overload phenomenon of semiconductor-insulator-semiconductor heterojunction caused by the ultra-thin interfacial layers

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The SIS (semiconductor-insulator-semiconductor) structure heterojunction derived from the MOS (metal-oxide-semiconductor) devices, and inherit the advantages of low cost, simple structure, stable performance and high theoretical efficiency, which drew tons of attention for solar cell and integrated circuit applications researches. SIS device consist of TCO (transparent conduction oxide) layer, ultra-thin oxide layer and silicon substrate, in which the carriers can tunnel through the oxide layer when the thickness of the interface oxide layer is reduced to 1–5 nm. Inside the SIS solar cell, the ultra-thin passivation layer has multiple functions including tunneling contact and buffer the crystalline lattice mismatch. Capacitance reflects a device's ability to charge and discharge, and the capacitance voltage (*CV*) characteristic is critical in the estimate of the passivation quality no matter in the high-low frequency method or DLTS (deep level transient spectroscopy system) method, and the passivation quality manifest as interface state density (D_{it}). When examining the high frequency (1 MHz) *CV* characteristic of the SIS which was fabricated by depositing ITO upon n-type silicon directly by RF magnetron sputtering, it is found that once the applied voltage (V_g) exceeds a certain value V_T (tunneling voltage), the differential capacitance value of the device would far beyond the range of the instrument and tends to infinity, which can be summarized as tunnel capacitance overload phenomenon (TCOP). As the description and explanation of this phenomenon have not been found in previous studies, the high-frequency TCOP of the SIS heterojunction with ultra-thin interfacial layers was investigated in details in this paper. The current-voltage characteristics of the SIS devices were obtained from the solar simulator and shown good photovoltaic conversion efficiency. The built-in electric field of the SIS with different ITO thickness was obtained by fitting the *CV* curves, which was measured by the Keysight E4980A *CV* system. The XPS depth profiling showed that the composition and percentage content of the interface, including In, Sn, O, Si, and the oxide silicon compound of Si_2O, SiO, Si_2O_3, SiO_2 which can be summed as SiO_x ($1 \leqslant x \leqslant 2$). The TEM images showed that the thickness of the SiO_x layer increases with the thickness of ITO layer, and the V_T in TCOP is apparently linked to the SiO_x thickness. When the applied V_g exceed V_T, a huge amount of electrons would enter the E_C of the silicon surface, unlike the MOS with thick and well passivated insulator layer, the ultra-thin SiO_x layer can't hold these mass of electrons at the SIS interface, so the electrons would directly tunnel through the SiO_x into the ITO layer and the TCOP appears. Capacitance voltage characteristics are critical for estimating the properties of heterojunction interfaces, and high frequency *CV* is indispensable for measuring the D_{it}. The existence of the TCOP is the main reason why other methods which based on the *CV* characteristics are difficult to estimate the interface state. But from another point of view, the TCOP is repeatable in the same device, which implied that the solar cells that fabricated by the directly depositing ITO thin films on n-type silicon is stable.

ultra-thin passivation layer, tunnel capacitance-voltagem, semiconductor-insulator-semiconductor, heterojunction, solar cell

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