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Citation: SCIENCE CHINA Information Sciences **54**, 1026 (2011); doi: 10.1007/s11432-011-4225-8

View online: https://engine.scichina.com/doi/10.1007/s11432-011-4225-8

View Table of Contents: https://engine.scichina.com/publisher/scp/journal/SCIS/54/5

Published by the Science China Press

SCIENCE CHINA
Information Sciences

• SPECIAL ISSUE •

May 2011 Vol. 54 No. 5: 1026–1038
doi: 10.1007/s11432-011-4225-8

RF/wireless-interconnect: The next wave of connectivity

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Received August 20, 2010; accepted October 13, 2010

Abstract In the era of the nanometer CMOS technology, due to stringent system requirements in power, performance and other fundamental physical limitations (such as mechanical reliability, thermal constraints, overall system form factor, etc.), future VLSI systems are relying more on ultra-high data rates (up to 100 Gbps/pin or 20 Tbps aggregate), scalable, re-configurable, highly compact and reliable interconnect fabric. To overcome such challenges, we first explore the use of multiband RF/wireless-interconnects which can communicate simultaneously through multiple frequency bands with low power signal transmission, reconfigurable bandwidth and excellent mechanical flexibility and reliability. We then review recent advances in RF/wireless-interconnect in four different potential application domains, which include network-on-chips (NoCs), 3-dimensional integrated circuit (3DIC), advanced memory interface and ultra-high speed contactless connectors. Based on those developments, we further propose the future research direction on future inter- and intra-VLSI interconnect system through the comparison of performance and the proper communication range for all three types of interconnects, including communication data throughput, range and power consumption (pJ/bit) among the RF/wireless-interconnects, the optical interconnects and traditional parallel repeated bus.

Keywords RF-interconnect, wireless RF-interconnect, network-on-chips, multi-band, 3-dimensional integrated circuit, advanced memory interface, wireless contactless connector

Citation Tam S W, Chang M C F. RF/wireless-interconnect: The next wave of connectivity. Sci China Inf Sci, 2011, 54: 1026–1038, doi: 10.1007/s11432-011-4225-8

1 Universal interconnect problems

Performance of future VLSI system is being limited by its interconnect bandwidth, power, performance and other fundamental physical limitations (such as mechanical reliability, thermal constraints, overall system form factor, etc.). Especially the interconnects in VLSI system, it has been predicted to be the ultimate limitation of the overall system performance in (as shown in Figure 1) consumer electronics [1–4], high speed connector [5], high speed memory interface [6] and future network-on-chip [7, 8]. Therefore, the interconnect system in future VLSI requires to have ultra-high data rates (up to 100 Gbps/pin or 20 Tbps aggregate), scalable, re-configurable, highly compact and reliable interconnect fabric. In order to adopt such rapid evolution in future interconnect in both on-chip and chip-to-chip communication, we explore the use of multiband RF/wireless-interconnects which can communicate simultaneously through multiple frequency bands with low power signal transmission, reconfigurable bandwidth and excellent mechanical flexibility and reliability.

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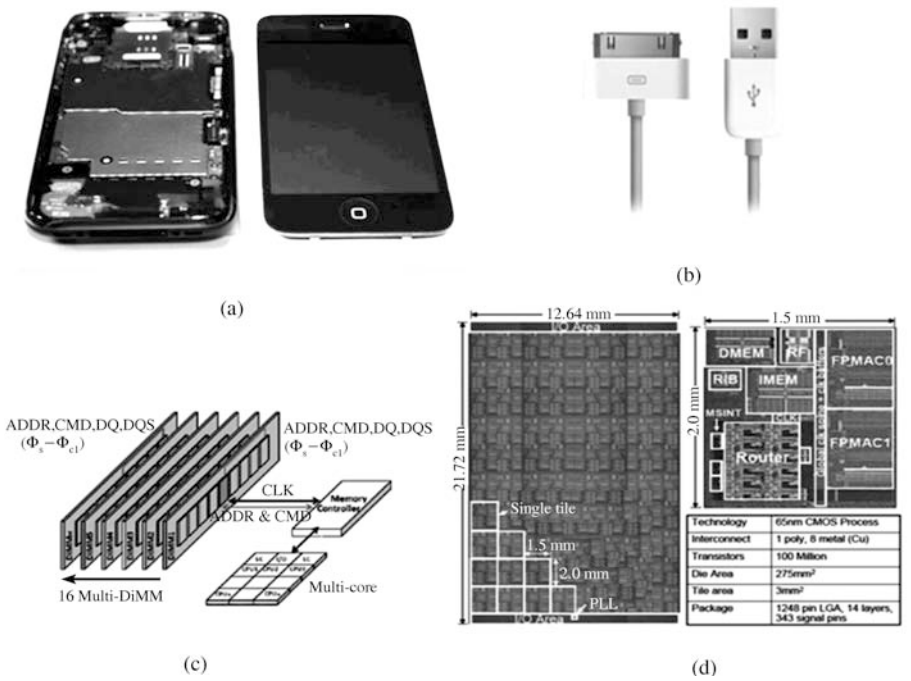

Figure 1 Interconnect becomes the ultimate limitation of the overall system performance in many systems such as consumer electronics (a), high speed connector (b), high speed memory interface (c) and future network-on-chips (d).

For example, in consumer electronics such as smartphones, the system drivers [1–4] are better performance/watt, lower cost and smaller in form factor. Due to the stringent requirement in form factor, traditional connectors for board to board or board to cable are not only bulky and speed-limited, but also suffer from poor mechanical reliability. By utilizing wireless RF-interconnect (WRF-I) technique, compact contactless connectors with ultra-high data rate and excellent mechanical properties become feasible.

In future network-on-chip (NoC)/chip-multiprocessors (CMPs), the contemporary solution to building many-core on-chip interconnects is the use of CMOS repeaters. However, despite improvements in transistor speed from one technology generation to the next, wire resistance and capacitance scale poorly, if at all. Figure 2(a) and (b) project the performance of a 2-cm on-chip repeater buffer link [8, 9] (i.e., a modern 2×2 cm^2 CMP inter-core interconnect) from 130 to 16 nm CMOS technology. These figures demonstrate that the link delay will grow worse with shrinking feature sizes and the scaling of energy per bit will be saturated at about 10 pJ/bit. Owens et al. [7] even predicted that at 22 nm technology, the total network power using repeater buffers will dominate CMPs power consumption. Consequently, future CMPs using the RC repeater buffer would encounter serious communication congestion and spend most of their time and energy in "talking" instead of "computing". Beside on-chip interconnect problems, off-chip interconnect such as memory interface is also a major limiting factor on the scaling of NoC/CMPs. Even though the number of pins in future micro-processors keeps increasing as well in each technology generation which is shown in Figure 3(a), the aggregate I/O bandwidth in the advance memory interface still cannot satisfy the future needs 0 without increasing the data rate of each individual I/O pin. Unfortunately, higher data rate requires more power to combat the lossy and dispersive channel with equalization circuit, and it hence increases the energy per bit and system complexity in each I/O pin, which is shown in Figure 3(b). With on/off-chip RF-interconnect (RF-I), higher data rates, lower power, scalable and re-configurable interconnect fabric can be achieved in future network-on-chip (NoC)/chip-multiprocessor (CMP).

In this paper, we first explore the use of multiband RF/Wireless-Interconnects which can communicate simultaneously through multiple frequency bands with low power signal transmission, reconfigurable bandwidth and excellent mechanical flexibility and reliability. We then review recent advances in RF/WirelessInterconnect in four different potential application domains, which include network-on-

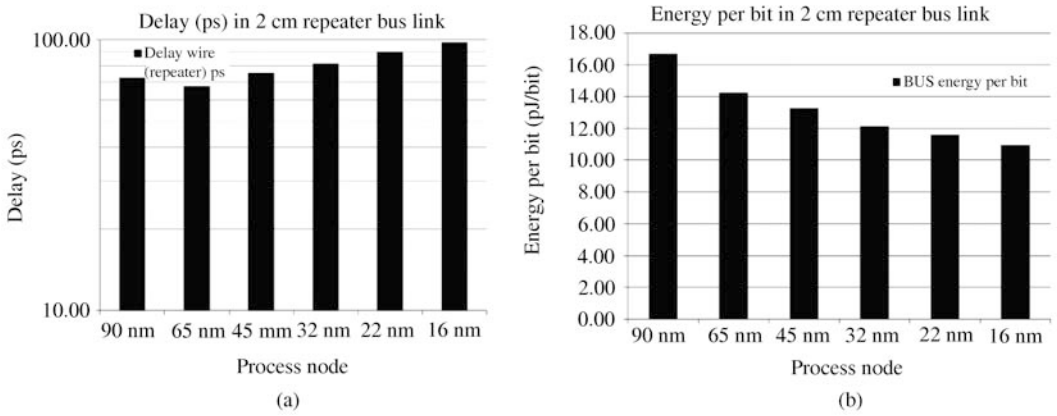

Figure 2 (a) Non-scalable delay of RC repeater buffer; (b) slow energy per bit scaling of RC repeater buffer.

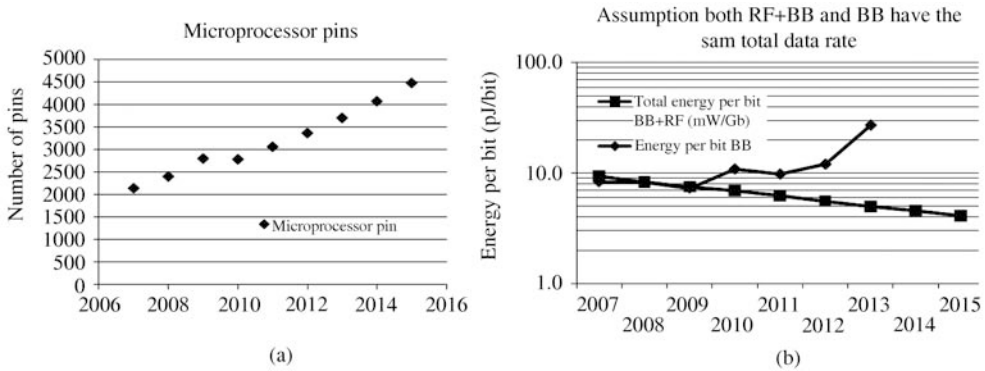

Figure 3 (a) Slow I/O pins scaling in microprocessor; (b) non-scalable energy per bit in off-chip baseband (BB) interconnect.

chips (NoCs), 3-dimensional integrated circuit (3DIC), advanced memory interface and ultra-high speed contactless connectors. Based on those developments, we further propose the research direction on future inter- and intra-VLSI interconnect system through the comparison on performance and the proper communication range for all three types of interconnects.

2 How can RF help on future inter- and intra-VLSI interconnect system?

One of the key benefits of the scaling of CMOS is that the switching speed of the transistor improves over each technology generation. According to ITRS [9], f_{T} and $f_{\max}$ will be 600 GHz and 1 THz, respectively, in 16 nm CMOS technology. A new record of a 324 GHz millimeter-wave CMOS oscillator [10] has also been demonstrated in standard digital 90 nm CMOS process. With the advance in CMOS mm-wave circuits, hundreds of GHz bandwidth will be available in the near future [11]. In addition, compared with CMOS repeaters charging and discharging the wire, EM waves travel in a guided medium at the speed of light which is about 10 ps/mm on silicon substrate. The question here is: How can we utilize over hundreds of GHz of bandwidth in a future VLSI system through RF-I/WRF-I?

One of the possibilities is to use multi-band RF-I based on frequency-division-multiple-access algorithms (FDMA) [12] to facilitate inter-core communications on-chip. In the past, we demonstrated on interconnect schemes both on-chip and 3DIC [13] that RF-interconnects can achieve high speed (5–10 Gb/s in 0.18 μm CMOS), low BER ($< 10^{-14}$ without error correction) [12, 14–18], seamless re-configurability, and simultaneous communications between multiple I/O users via multiple frequency bands by using shared physical transmission lines. The main advantages of RF-I include:

• Superior signal to noise ratio. Since all data streams are modulated by RF-carriers, which are at least 10 GHz above the baseband, the high speed RF-interconnect does not generate and/or suffer from any baseband switching noise.

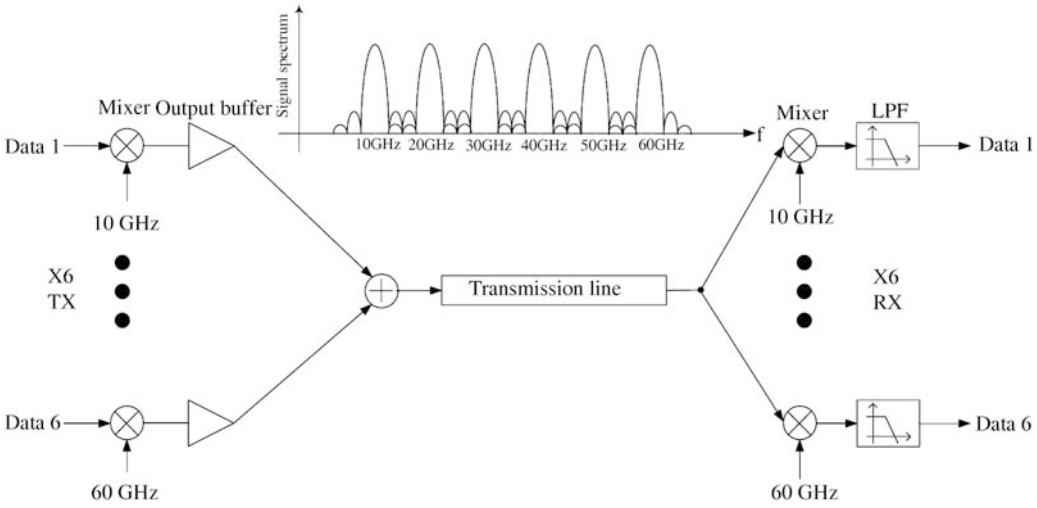

Figure 4 Conceptual schematic of the multi-band RF-interconnect with six RF carriers.

• High bandwidth. A multi-band RF-interconnect link has a much higher aggregate data rate than a single repeater buffer link.

• Low power. Compared to a repeater buffer, a multi-band RF-interconnect is able to operate at much better energy per bit.

• Low overhead. High data rate/wire and low area/gigabit and low latency due to speed-of-light data transmission.

• Re-configurability. Efficient simultaneous communications with adaptive bandwidths via shared on-chip transmission lines.

• Multicast support. Scalable means to communicate from one transmitter to a number of receivers on chip

• Total compatibility and scalability. Both RF-I/WRF-I are implemented in mainstream digital CMOS technology

The concept of RF-I is based on transmission of waves, rather than voltage signaling. When using voltage signaling in conventional RC time constant dominated interconnects, the entire length of the wire has to be charged and discharged to signify either '1' or '0'. In the RF approach, an electro-magnetic (EM) wave is continuously sent along the wire (treated as a transmission line) or over on-chip antenna. Data is modulated onto that carrier wave using amplitude and/or phase changes. By expanding the idea of the single carrier RF-I, it is possible to improve bandwidth efficiency using N-channel multi-carrier RF-I. In multi-carrier RF-I, there are N mixers in the Tx. Each mixer up-converts individual base-band data streams into a specific channel. Those N distinct channels transmit N different data streams onto the same transmission line. The total aggregate data rate (R_{Total}) equals to $R_{\text{Total}} = R_{\text{baseband}} \times N$, where the data rate of each base-band is R_{baseband} and the number of channels is N. A conceptual illustration of a six-carrier FDMA RF-interconnect is shown in Figure 4.

3 Overview on recent advances in RF/wireless-interconnect

3.1 Network-on-chip

In this section, we first illustrate the implementation of a simultaneous tri-band on-chip RF-interconnect to demonstrate the feasibility of multi-band RF-interconnect for future network-on-chip. Furthermore, we propose a micro-architectural framework that can be used to facilitate the exploration of scalable low power NoC architectures based on physical planning and prototyping.

The schematic of the proposed tri-band RF-I [16] is shown in Figure 5. The modulation scheme of each RF band is amplitude-shift keying (ASK), in which a pair of on-off switches directly modulates the RF carrier. The baseband (BB) utilizes a low-swing capacitive coupling interconnect technique. The

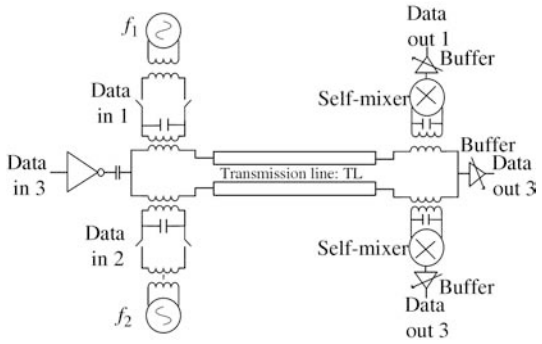

Figure 5 Schematic of the on-chip tri-band ASK RF-I.

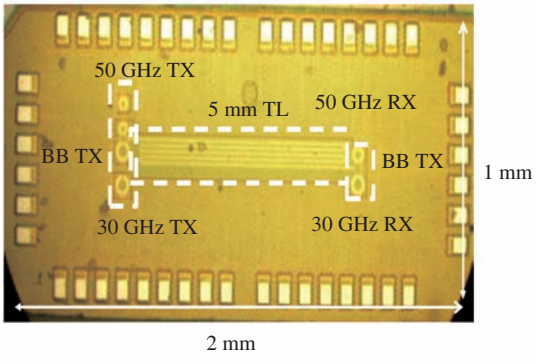

Figure 6 Die photograph of the tri-band on-chip RF-I based on 90 nm IBM CMOS.

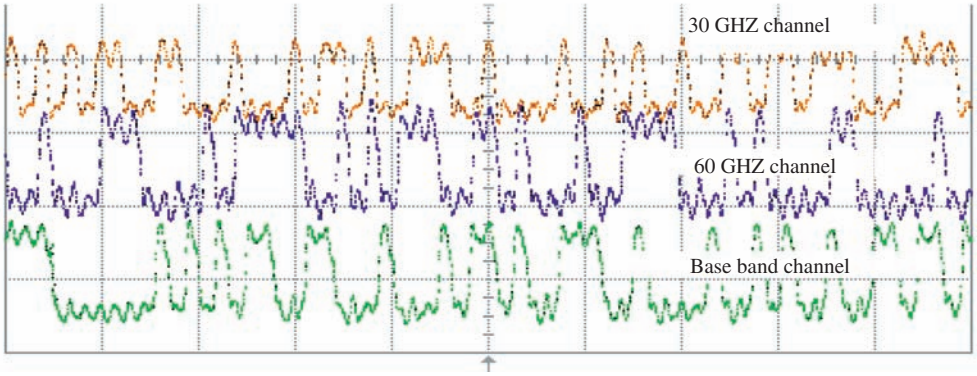

Figure 7 Data output of the tri-band waveform 30 GHz, 50 GHz and base band.

baseband data is transmitted and received using the common mode of the differential transmission line (TL). At low frequencies, the transformer becomes a short circuit, and a pair of low-swing capacitive coupling buffers transmits and receives the baseband data at the center tap of the transformer. The transmitter and the receiver are connected by an on-chip 5 mm long differential TL. In order to support simultaneous multi-band RF-I on a shared TL, RF band and BB are transmitted in differential mode and common mode, respectively. These two propagation modes are naturally orthogonal to each other and suppress the inter-channel interference (ICI) between RF band and BB.

The tri-band on-chip RF-I is implemented in the IBM 90 nm digital CMOS process. The die size is 1 mm×2 mm, as shown in Figure 6. Figure 7 shows the recovered data waveform of the 3 bands: 30 GHz, 50 GHz and BB. The maximum data rates for each RF band and BB are 4 and 2 Gb/s, respectively. The total aggregate data rate is 10 Gb/s. A RF-I with TX and TL only was also implemented for measuring the spectrum of the tri-band RF-I signals. A 67-GS cascade micro-probe directly probes the on-chip differential TL (only differential mode can be measured). Figure 8(a) shows the free running VCO spectrum without input data modulation on both RF bands at 28.8 and 49.5 GHz respectively. When the two uncorrelated 4 Gb/s random data streams are applied to both RF bands, as shown in Figure 8(b), the spectrum of each band broadens and spreads over 10 GHz of bandwidth. The tri-band RF-I achieves superior aggregate data rate (10 Gb/s), latency (∼6 ps/mm) and energy per bit (0.09 pJ/bit/mm and 0.125 pJ/bit/mm, for RF and BB, respectively). The measured BER across all channels is $< 1 \times 10^{-9}$. As the RF band approaches to the maximum data rate, BER of RF bands starts to degrade while BB remains unchanged.

While RF-I has dramatic potential in terms of low-latency, low-power, high-bandwidth operation, the key enabling component of RF-I for future microprocessor architectural design is re-configurability. As an example of this re-configurability, we recently proposed MORFIC (mesh overlaid with RF inter-connect) [14, 15], a hybrid NoC design which is shown in Figure 9. It is composed of a traditional mesh of routers

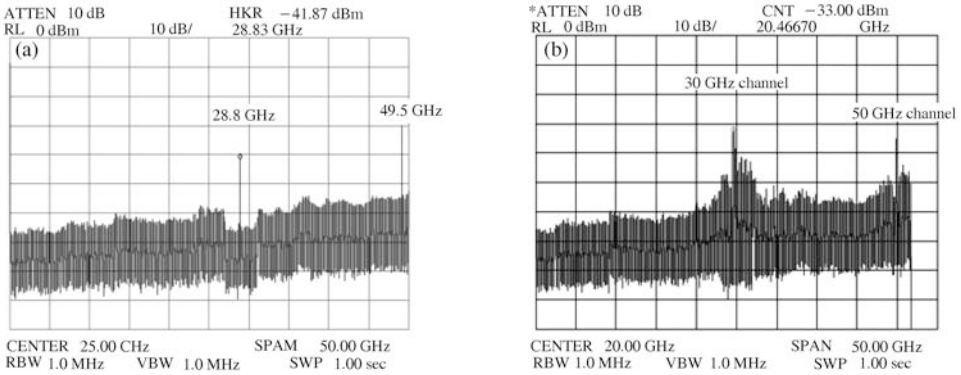

Figure 8 Spectrum on the differential mode RF-I signal with (a) no data input; (b) with 4 Gbps data input in each band.

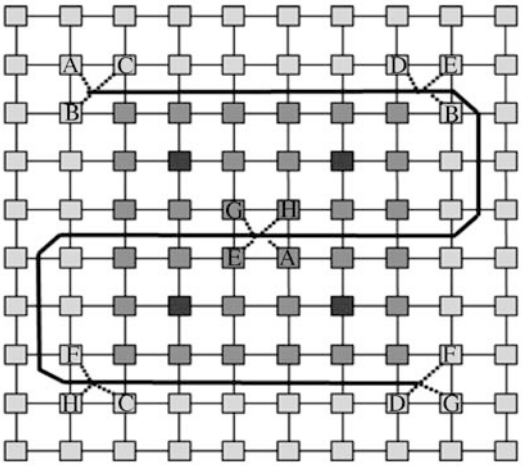

Figure 9 Schematic of MORFIC.

augmented with a shared pool of RF-I that can be configured as short-cuts within the mesh. In this design, we have 64 computing cores, 32 cache memory modules and 4 memory output ports, and RF-I is a bundle of transmission lines spanning the mesh, and features 16 carrier frequencies. We examined four architectures: 1) Mesh Baseline—a baseline mesh architecture without any RF-I; 2) Mesh Wire Baseline—the baseline mesh architecture with express shortcuts between routers (conventional wire, not RF-I) that are chosen at chip design time (i.e. no adaptability to application variation); 3) Mesh Static Shortcuts—the same express shortcuts as the Mesh Wire Baseline but using RF-I instead of conventional repeated wire; and 4) Mesh Adaptive Shortcuts—the overlaid RF-I with shortcuts tailored to the particular application in execution. From the simulation results of our in-house cycle-accurate simulator [19], we demonstrated a significant performance improvement of the Mesh Adaptive Shortcuts over the Mesh Baseline, an average packet latency reduction of 20%–25% [14], through the reconfigurable RF-I, as shown in Figure 10(a). We further demonstrated a 65% power reduction [20] by reducing the bandwidth of the baseline mesh by 75%—reducing the 16 Byte wide to 4 Byte wide baseline mesh, as illustrated in Figure 10(b). Our continued exploration of the MORFIC architecture will be instrumental in gauging future CMP interconnect design tradeoffs, and in better quantifying what benefits CMPs can expect from MORFIC in future generations of CMOS technologies down the road.

3.2 3-Dimensional integrated circuit

One of the current technological trends in CMOS processes is 3-dimensional (3D) stacking [21], in which several thin tiers of circuitry are stacked vertically to achieve a higher level of integration. Due to vertical integration, the same functionality can be implemented in a smaller chip area, reducing both cost and the distance signals required to travel across the chip. Reduced distance decreases both transmission

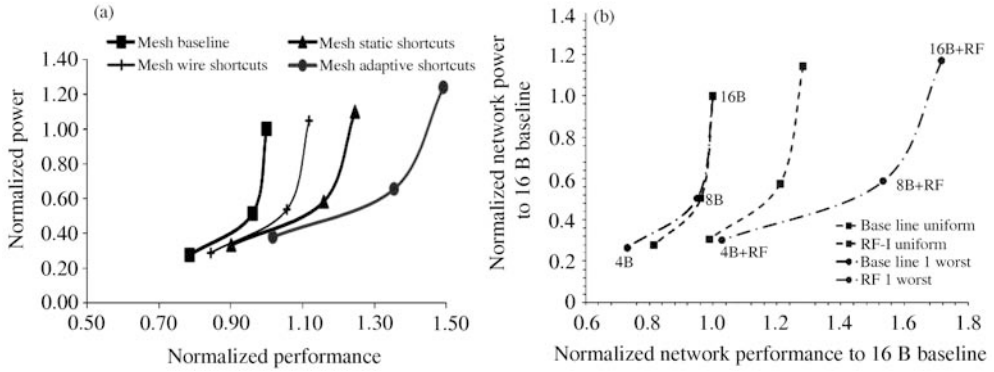

Figure 10 (a) Power performance trade-off curve of the mesh adaptive shortcuts over the mesh baseline; (b) power performance trade-off curve on different baseline mesh bandwidth from 16 Byte wide to 4 Byte wide baseline mesh.

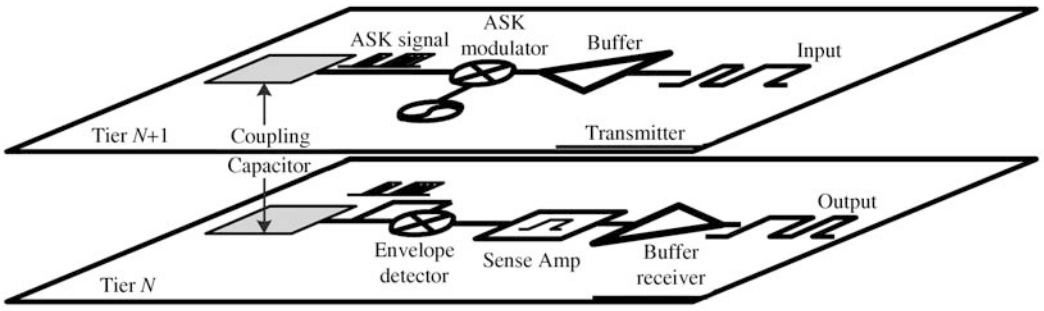

Figure 11 Schematic of the RF-interconnect implemented in a 3D 0.18 μm CMOS process.

latency and the consumed energy. However, 3D stacking requires vertical connection between transistor and metal tiers, usually implemented using metal studs that cut through layers of silicon and insulators. Alignment of such direct connection is difficult on a large scale and therefore requires a relatively large connection area.

The use of RF signaling has an advantage over standard voltage signaling for inter-layer communication. Because the signal is modulated on a high-frequency carrier, it does not require a direct connection, and capacitive or inductive coupling is enough for transmission. Figure 11 shows a schematic view of a fabricated 3DIC demonstrating an RF-I using capacitive coupling [13], with the photograph of the actual die shown in Figure 12(a). In this circuit implemented in 180 nm 3D SOI processed provided by the MIT Lincoln Lab, an amplitude shift keying (ASK) modulation of a 25 GHz carrier is used so that recovery of the data requires only an envelope detector. Metal layers in each of the tiers are used to form capacitors with values of tens of femto-farads that are sufficient for effective coupling. This realized RF interconnect achieves a maximum data rate of 11 Gb/s per wire and a very low BER of 10^{-14} measured at about 8 Gb/s, as shown in Figure 12(b). The use of small capacitors for coupling has an advantage over on-chip inductors or antennas due to the better field confinement that reduce cross-talk and interference between differential links.

3.3 Advanced RF-I memory interface

As the required aggregate data rate of the off-chip high speed I/O link such as memory interface keeps increasing [5], the overall power consumption and total number of I/O pins have been increasing as well, and such stringent design requirements eventually become the ultimate bottleneck of the overall system. For example, current high speed memory interface design resolves this problem by only increasing the speed of baseband I/O interfaces while ignoring the ever increasing in power consumption and system complexity. Therefore, we propose a multiband low power RF-I memory interface system that can support multiband and reconfigurable data communication by adding multiple lower energy per bit RF bands

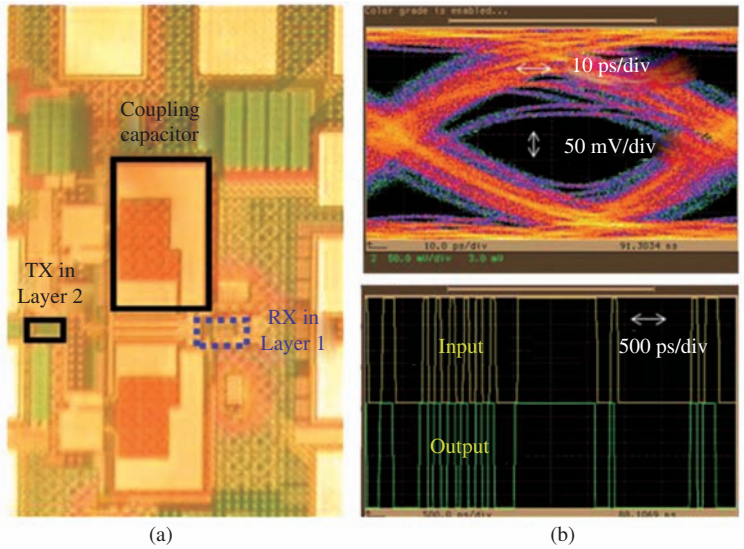

Figure 12 (a) Chip photograph of 3D RF-interconnect; (b) measurement result of the 3D RF-Interconnect at 11 Gbps with 2^{15}-1 PRBS.

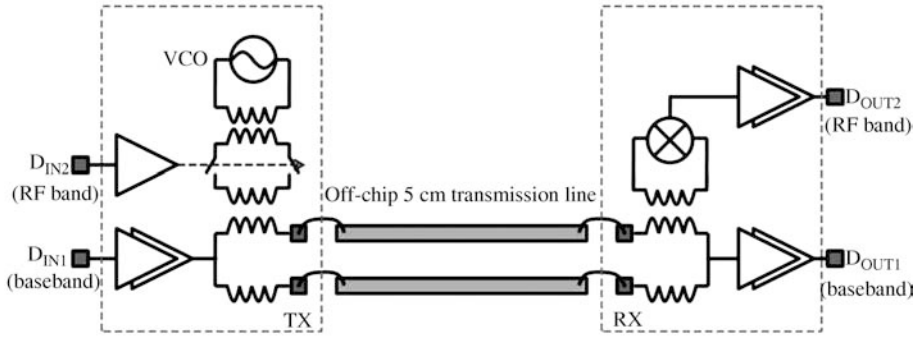

Figure 13 Schematic of the advanced RF-I memory interface system.

on top of existing baseband high speed memory interface such as DDR2 or DDR3. This new proposed memory interface is not only able to maintain relatively low baseband data-rate with manageable power consumption, but it is also able to achieve ultrahigh aggregate data-rate with less number of I/O pins to meet future fast growing data throughput demand in memory interface.

In order to demonstrate this new concept, we implemented a simple prototype of the advanced RF-I memory interface [18] which is shown in Figure 13. This simple prototype is implemented together with the conventional baseband (BB) DDR2 memory interface and RF transceivers which enable simultaneously BB and RF-band (25 GHz RF carrier) communication over a shared parallel transmission line on the printed circuit board. This advanced RF-I memory interface transceiver chip is fabricated in a 65 nm digital CMOS technology, and the chip microphotograph is shown in Figure 14. The test board with dual chips achieves a total data rate of 10 Gb/s/pin over a 5 cm RO4003 differential transmission line. Figure 15(a) and (b) show the measured data eye diagram with a BER of 10^{-9} and 10^{-10} for the RF and baseband, respectively.

3.4 Ultra-high speed contactless connector

In this section, a technique using wireless RF interconnect (WRF-I) [17] with asynchronous ASK modulation scheme is utilized for multi-gigabit ultra short distance (less than 10 cm) chip to chip or board to board contactless connector. WRF-I transmits the data over the air in a very short distance (10 cm or less) without any physical contact, in contrast to conventional high speed broad to broad connector, which is lossy and poor in mechanical properties. The main advantages of WRF-I include high data rate,

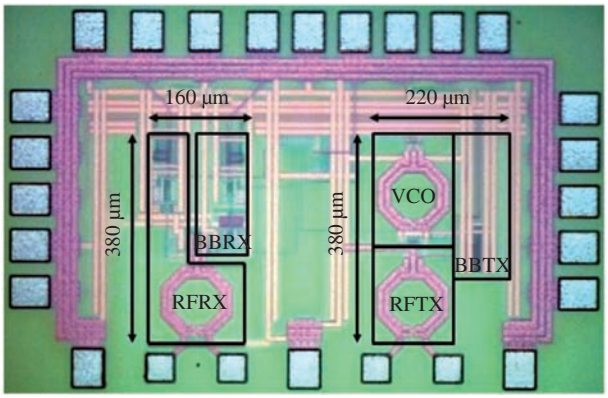

Figure 14 Chip microphotograph of the advanced RF-I memory interface system.

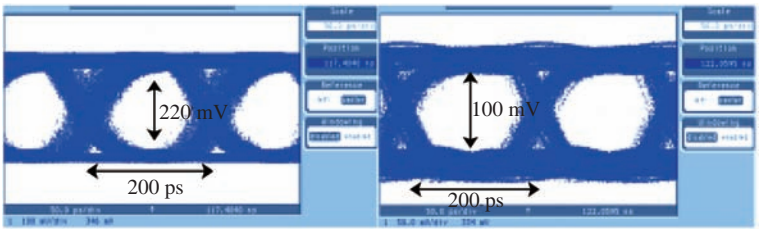

Figure 15 Measured 10 Gb/s/pin data eye diagram: (a) 5 Gb/s RF (25 GHz RF carrier); (b) 5 Gb/s BB.

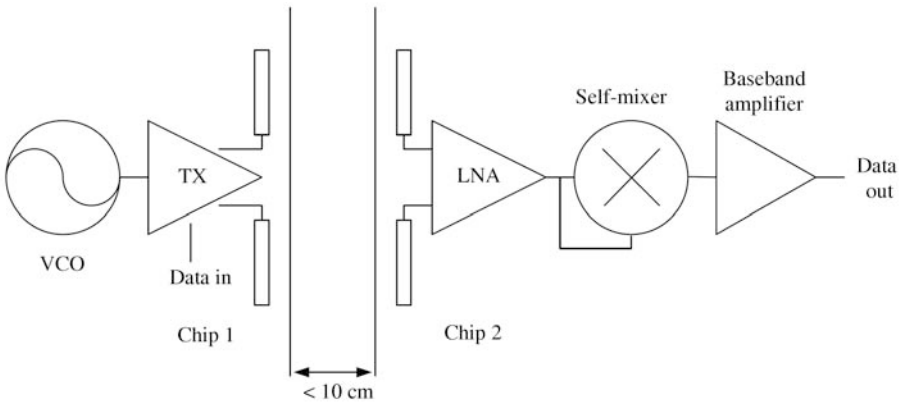

Figure 16 Schematic of a single channel wireless RF-I using on-chip antenna.

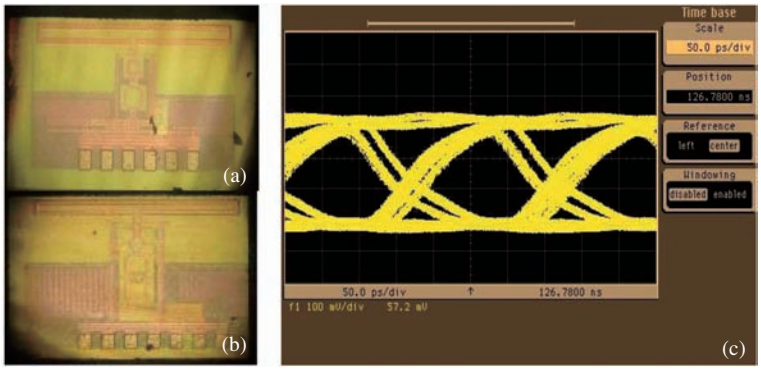

Figure 17 (a) and (b) Chip microphotograph WRF-I transceiver; (c) measured 5 Gb/s/channel data eye diagram.

re-configurability, low power, scalability, no mechanical contact and reduction on broad to broad connector complexity.

The transmitter first modulates the RF-carrier with the input data stream, and then further amplifies to higher power level. The modulated RF-carrier is then fed to the antenna and radiated to air. At the end, the receiver antenna receives the radiation from transmitter antenna and converts received signal to full swing digital signal. By choosing the RF-carrier in mm-wave frequencies, the higher carrier to data rate ratio further minimizes the dispersion of the signal and removes the need for a power hungry equalization circuit. Moreover, the size and signal loss of antenna are both dramatically reduced in mm-wave frequencies. In such short distance communication (less than 10 cm), the design requirements of antenna such as antenna gain, directivity, radiation efficient and power matching are greatly relaxed. Figure 16 shows the schematic of a single channel wireless RF-I using on-chip antenna.

Single channel WRF-I can be further expanded to multiple channels. By placing every two transceivers in alternating fashion at the edge of printed circuit board (PCB), which operate in two different carrier frequencies, N channels of WRF-I for board to board communication is possible. In this multi-channel WRF-I, the isolation between adjacent channels is the key. The aggregate data rate across two PCBs is $N \times BW$, where N is total number of channel and BW is bandwidth of each transceiver.

The single carrier WRF-I is implemented in the TSMC 65 nm digital CMOS process, and the chip microphotograph of the transmitter and receiver are shown in Figure 17(a) and (b) respectively. Figure 17(c) shows the recovered 5.7 Gbps data waveform with carrier frequency at 60 GHz and 5 mm separation distance. The measured BER across all channels is $< 1 \times 10^{12}$ and the energy per bit is 8 pJ/bit.

4 Future research directions

In this final section, we compare the performance and the proper communication range for all three types of interconnects, including the traditional parallel repeated wire bus, the RF-I and the optical interconnect. We first compare the latency, the energy consumption per bit and the data rate density among them in Figure 18 for the same 2-cm communication distance on-chip. The performance of the parallel repeater bus is projected according to the ITRS digital technology roadmap [9] with optimized repeater design practice; the RF-I performance is estimated based on the RF-technology roadmap, employing our proposed RF-I design methodology portrayed above. The optical interconnect performance is calculated based on [22–24] and extrapolated to further scaled technology nodes. In contrast to the latency increase of the traditional repeater bus against the scaling shown in Figure 18(a), RF and optical interconnects are able to maintain similarly low latency over the scaling and keep the 2 cm data transmission within a clock cycle. The RF and optical interconnects again show significant benefit in energy consumption over the traditional bus, as shown in Figure 18(b). The RF-I even scales slightly better than that of optical interconnect in terms of absolute energy per bit. Data rate density is expected to improve in all three interconnects: the bus would benefit from the wire pitch; RF-I benefits from the number of carrier bands and the effective transmission speed possible; and the optical data density should improve under the assumption of more wavelengths used, although its optical transceiver typically requires non-CMOS devices which are less scalable due to fundamental physical constraints and often more sensitive to temperature variations. RF-I, on the other hand, has the major advantage of using the standard digital CMOS technology.

Besides the performance, we may also assess the optimized communication range for each of the interconnect technologies. As CMOS continues to scale toward 16 nm, traditional on-chip RC repeated wires are more suitable for local interconnects with short communication distance due to further increased physical density through the use of minimum-feature-width metal wires [8]. Figure 19(a) illustrates the projected power/performance of both RC wires with optimal delay and RF-I with a 16 nm CMOS process [9]. Under approximately 1 mm, the RC repeater is able to provide superior energy efficient communication, but beyond 1 mm, the repeater buffers become less efficient than those of RF-I. The RF-I is expected to maintain its performance advantages for global interconnect on-chip due to its total compatibility with the CMOS technology, but can it maintain the same superiority to an extended distance off-chip? Especially, to what range can it compete with the optical interconnect which is clearly

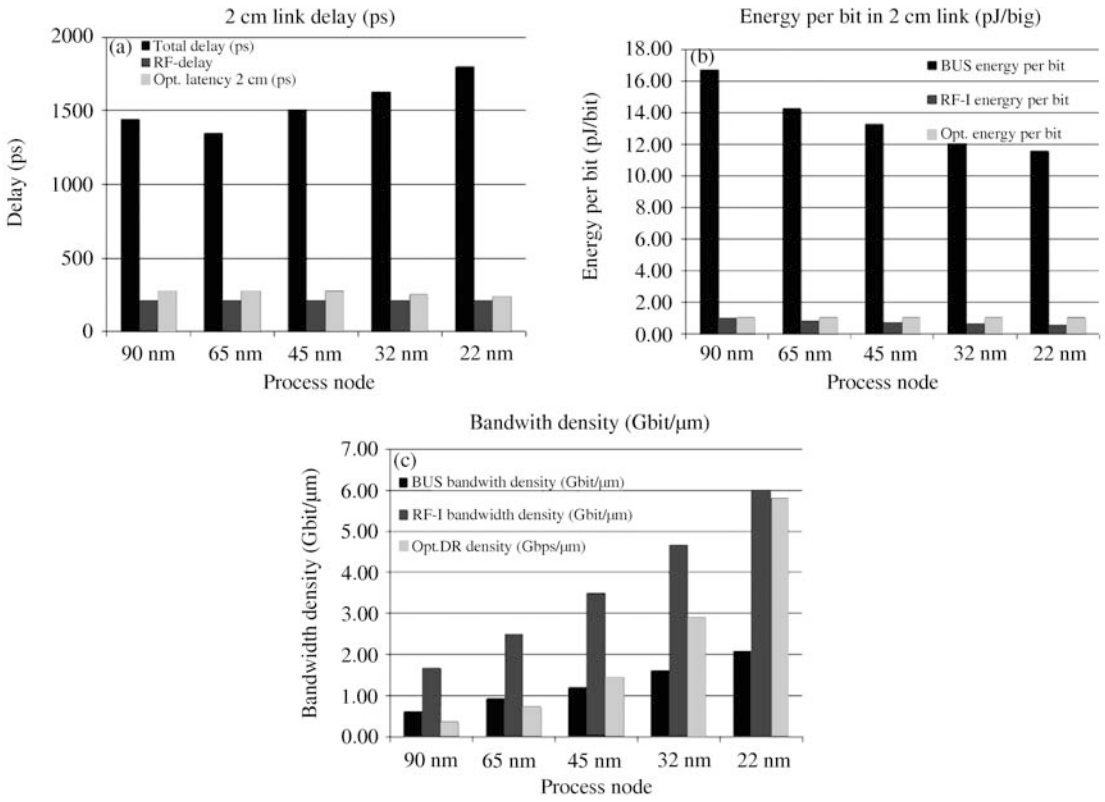

Figure 18 Comparison of interconnect technologies for a global 2 cm (a) on-chip distance of latency, (b) energy consumption per bit and (c) data rate density for a traditional repeated parallel bus, RF-I and optical interconnect.

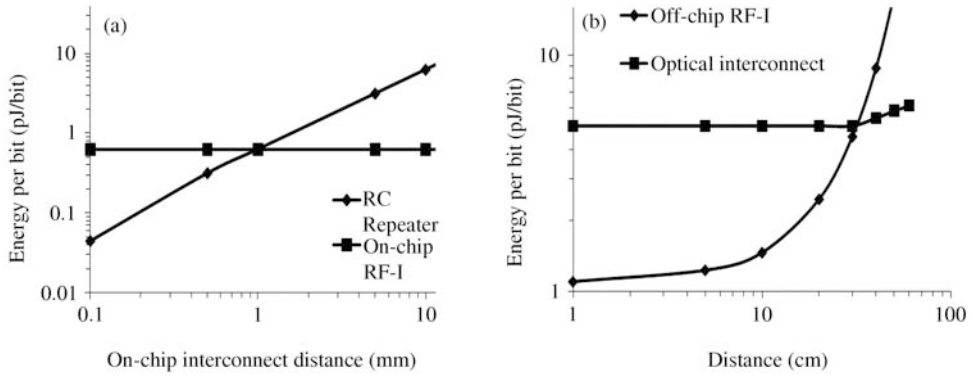

Figure 19 (a) RF-I will crossover the energy efficient curve of the RC repeater, and become more energy efficient above a 1 mm interconnect distance at a 16 nm CMOS process; (b) RF-I has much better energy efficiency in the mid-range distance of 30 cm or below, while the optical interconnect does not have any benefit until an interconnect distance over 30 cm.

superior for longer-distance communications? We offer the answer to those questions by comparing the energy efficiency between the off-chip RF-I and optical interconnect in Figure 19(b), where the off-chip RF-I energy-per-bit is estimated with the physical transceiver/transmission line designs based on [16], and the optical interconnect results are obtained through the data from [22–24]. Accordingly, the RF-I actually exhibits better energy efficiency at mid-range distances of 30 cm or below. As the communication distance increases, RF-I energy efficiency decreases rapidly due to the excessive power required to compensate for the severe loss from the on-board transmission lines, while the power consumption of optical interconnect remains almost constant. Therefore, despite substantial disadvantages in integration and cost, the optical interconnect becomes more beneficial at interconnect distances beyond 30 cm. That is to say, in between

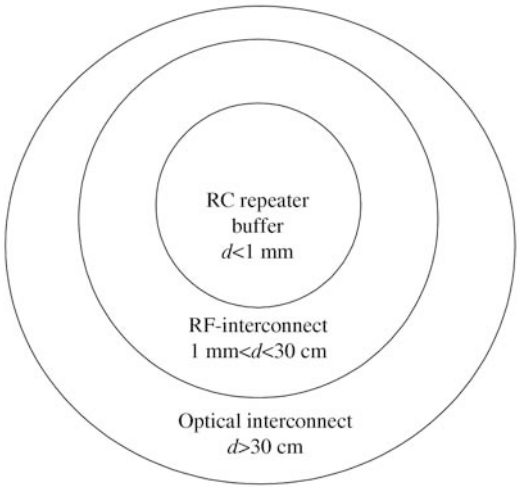

Figure 20 Communication range versus interconnect technologies as CMOS process continuously to scale toward 16 nm.

traditional RC repeater buffer and optical interconnects, there is an obvious technology gap for achieving cost/performance-effective communications in mid-distance range from a few millimeters to several tens of centimeters. The CMOS compatible RF-I may be the right technology to fill in such a technology gap, as shown in Figure 20, with the lowest latency, the least energy consumption, and the highest data rate density.

Acknowledgements

The authors would like to thank US DARPA and GSRC for their contract support and TAPO/IBM, TSMC and MIT Lincoln Lab for their foundry services.

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