SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

February 2014, Vol. 57 022402:1–022402:13
doi: 10.1007/s11432-013-4902-x

Low power adiabatic logic based on FinFETs

LIAO Nan, CUI XiaoXin*, LIAO Kai, MA KaiSheng, WU Di,
WEI Wei, LI Rui & YU DunShan

Institute of Microelectronics, Peking University, Beijing 100871*, China*

Received January 18, 2013; accepted May 28, 2013

Abstract With the aggressive scaling of device technology, the leakage power has become the main part of power consumption, which seriously reduces the energy recovery efficiency of adiabatic logic. In this paper, a novel low-power adiabatic logic based on FinFET devices has been proposed. Due to the lower leakage current, higher on-state current and design flexibility of FinFETs, the proposed adiabatic logic shows considerable power reduction, performance improvement and area saving compared with CMOS adiabatic logic. An 8-state clock chain as the test circuit has been demonstrated based on the 32-nm FinFET Predictive Technology Model. The simulation results show that adiabatic circuit based on FinFET devices achieves a power reduction of up to 84.8% and a limiting frequency of up to 55 GHz.

Keywords leakage power, FinFET, adiabatic logic, power reduction, limiting frequency

Citation Liao N, Cui X X, Liao K, et al. Low power adiabatic logic based on FinFETs. Sci China Inf Sci, 2014, 57: 022402(13), doi: 10.1007/s11432-013-4902-x

1 Introduction

In recent years, the rapid development of transistor technology has resulted in higher performance and integration density. Simultaneously, the continuous increasing power has become the primary barrier against further development of VLSI circuit design. Power consumption is composed of two parts: dynamic power and static power. The dynamic power is due to the switching activities during charging and discharging process, while static power is caused by the inherent device leakage when the circuit is in the off state [1]. Therefore, both dynamic power and static power need to be investigated in the low-power VLSI circuit design.

In early period, the power consumption was once dominated by the dynamic power. A lot of novel circuit technologies like adiabatic circuit [2], sub-threshold circuit [3] and multi-threshold technology [4] have been introduced to reduce dynamic power. Among these, adiabatic logic, a novel low-power circuit structure, utilizes AC voltage supply rather than DC voltage supply to recycle the energy of circuits. This method forces the node voltage to vary synchronously with the power supply; as a result, the energy stored in the node capacitance is only 0.5 CV^2, which avoids the heat dissipation in charging and discharging period. Furthermore, the energy stored can flow back to the voltage supply when the supply

*Corresponding author (email: cuixx@pku.edu.cn)

recovers to zero. Theoretically, zero power consumption can be realized by the adiabatic logic without considering the leakage power.

In recent years, there have been intensive researches on low power adiabatic logic. A 32×32 register file based on dual transmission gate adiabatic logic that could be applied to a larger memory and reduce the energy dissipation is presented in [5]. Samson and Mandavalli [6] proposed an energy efficient and high density adiabatic 5T SRAM that can achieve 98% power reduction when compared with 6T conventional SRAM. Ultra low-power adiabatic sequential circuits like D, JK, T flip-flops are explored in [7]. Besides, it was reported that the adiabatic logic styles have better differential power analysis (DPA) resistances than the conventional CMOS logic [8,9].

However, with the aggressive scaling of device technology and threshold voltage, the leakage current has increased significantly, becoming the main part of power consumption [10]. It is hard to realize efficient bulk CMOS adiabatic logic due to the large leakage current. Hence, it is necessary to investigate novel devices to reduce the leakage power. Among the novel devices, FinFET device, a special quasi-planar double-gate device, has been proposed as a promising alternative for addressing the challenges brought by the continued scaling [11]. This device demonstrates excellent performance and low-power characteristic. It can well suppress the Short-Channel Effects (SCEs) and the gate-dielectric leakage current. Meanwhile, the double gates of a FinFET device can be controlled independently, which increases the design flexibility.

FinFET circuit design has become one of the major means which focuses in low-power systems design [12]. Recently an independent-double-gate (IDG) FinFET SRAM has been successfully fabricated with considerable reduction of not only leakage current but also the dynamic power consumption by appropriately controlling the $V_{\rm th}$ of the IDG-FinFET [13]. Three novel independently-controlled-gate Schmitt Trigger (IG_ST) 8T FinFET SRAM cells for sub-threshold operation are proposed in [14]. The proposed cells can provide better Read Static Noise Margin (RSNM) , higher density, and lower standby leakage current than conventional 10T Schmitt Trigger sub-threshold SRAM cells. Jafari et al. have proven that FinFET is a promising technology for designing robust and power efficient asynchronous circuits [15]. A novel FinFET based domino logic is presented in [16]. Its logic shows higher performance and lower power consumption than standard domino logic, which is beneficial in high fan-in logic. Besides, a synthesis scheme based on threshold control through multiple supply voltages (TCMS) was proposed to reduce both power consumption and devices area [17].

Up to now, no researches in literature are available on FinFET adiabatic circuit. This paper proposes some adiabatic logics based on FinFET devices to reduce the power consumption. Four types of adiabatic logics, i.e. 2N2N2P logic [18], improved pass-transistor adiabatic logic (IPAL) [19], positive feedback adiabatic logic (PFAL) [20] and differential cascode pre-resolve adiabatic logic (DCPAL) [21], are restructured by Short-Gate mode FinFET, Low-Power mode FinFET and Independent-Gate mode FinFET respectively. Simulations are conducted on an 8-state adiabatic clock chain for demonstration. All the simulations are based on predictive technology model (PTM) for 32-nm FinFETs and 32-nm CMOS [22].

2 Background

2.1 Adiabatic logic

Conventional static CMOS circuits suffer the inevitable energy loss ($\mathrm{CV}_{\mathrm{DD}}^2$) at each charging and discharging operations. In the charging operation, the energy dissipation from power supply through pull-up PMOS block is $\mathrm{CV}_{\mathrm{DD}}^2$. $0.5\mathrm{CV}_{\mathrm{DD}}^2$ energy is stored in load capacitance. The other half of the energy is dissipated in the resistive path, and converted to heat. During the discharging operation, the residual $0.5\mathrm{CV}_{\mathrm{DD}}^2$ energy stored in the capacitance is released through pull-down NMOS block to the ground terminal. Therefore, no energy can be recovered in the conventional CMOS circuit.

Adiabatic circuits employ AC power source (clock) rather than the DC supply, and therefore can recover the energy stored in capacitance back to the power source, and completely avoid the dynamic power dissipation theoretically. In adiabatic logic, the node voltage changes synchronously with the

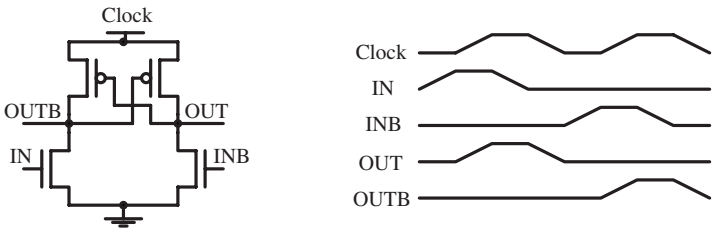

Figure 1 2N2P buffer and the corresponding time sequence.

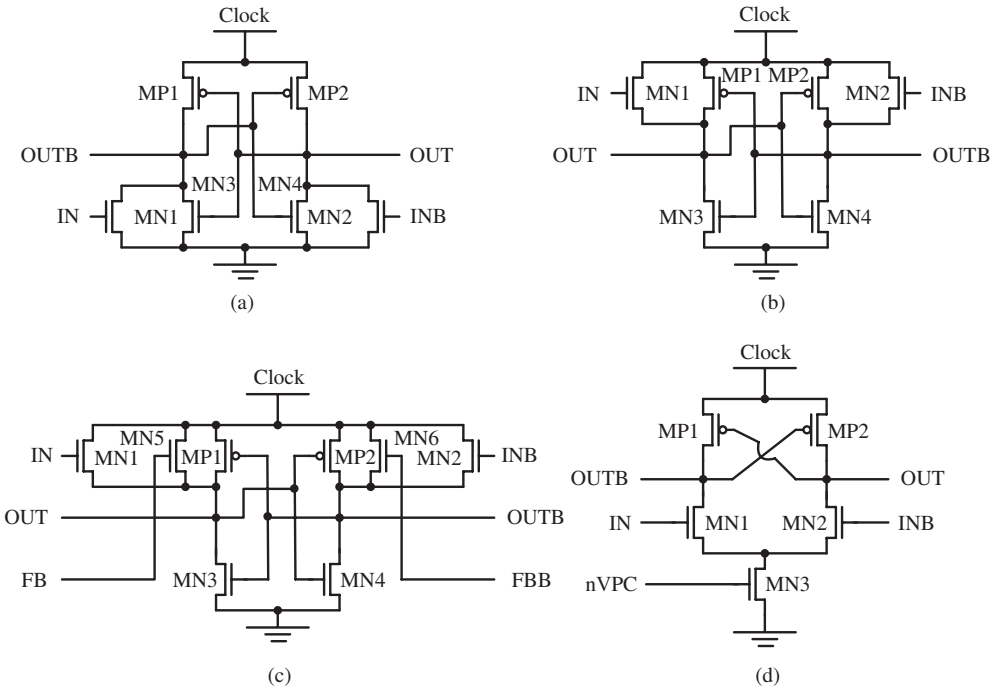

Figure 2 Four conventional four-phase adiabatic buffers. (a) 2N2N2P; (b) IPAL; (c) PFAL; (d) DCPAL.

supply voltage (sine wave); thus the energy released from the power supply is just 0.5 CV_{DD}^2, which could be stored in the load capacitance. Moreover, when the supply voltage falls down to the ground level, the energy stored in the capacitance could flow back to the power supply. Therefore in the field of low power design, adiabatic logic is a good selection in the circuit level.

Usually the adiabatic circuit operation consists of four phases, namely Wait, Evaluate, Hold and Recover. The phase difference between adjacent phases is a quarter of period. Here in Figure 1, the simplest adiabatic buffer with 2N2P structure, which contains two cross-coupled P-MOSFETs and two differential input N-MOSFETs, is taken as an example to explain the four-phase operation mode [23]. The N-MOSFETs block is the evaluation logic and the P-MOSFETs are the charging and discharging current access of the adiabatic logic. The typical time sequence of the 2N2P logic is also shown in Figure 1. The four-phase operations are shown as follows:

1) Wait: The power supply stays zero, the inputs become valid and the evaluation logic generates pre-evaluated result and the outputs keep low voltage.

2) Evaluate: The power supply rises from zero to V_{DD} gradually, and inputs remain stable. According to the result of pre-evaluation, output follows the power supply to become valid.

3) Hold: The power supply stays high to keep the output valid, providing the constant input signal for the next stage in the adiabatic pipeline. Besides the inputs return to zero.

4) Recover: The power supply climbs down to zero. The remaining zero voltage inputs shut down the current access to the ground; thus the charge stored in the node capacitance can flow back to the power supply through the cross-coupled P-MOSFETs.

The most widely used adiabatic logics include 2N2N2P, IPAL, PFAL and DCPAL. Above four types adiabatic buffers are shown in Figure 2. They have similar operations with 2N2P logic but also have some differences. In the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple, which increases the stability of the outputs. The IPAL logic folds the evaluation logic upward to the pull-up blocks to form two charging paths with a pair of cross-coupled P-MOSFTEs, which reduces the time taken to evaluate the outputs. Based on the IPAL logic, The PFAL logic adds a pair of feedback N-MOSFETs, and the feedback signal comes from the next stage's outputs. This structure effectively eliminates the charge stored in the output node after the recovery phase, which can provide complete charge recovery. DCPAL adds a gating N-MOSFET in the pull-down path to reinforce the suppression of leakage current.

To sum up, considerable dynamic power reduction can be realized by adiabatic circuit. However, with the aggressive scaling of devices technology, the leakage power becomes more and more serious. Hence, leakage current should be carefully considered in the adiabatic circuit design.

2.2 FinFET device

FinFET has a three-dimensional structure. It consists of a thin silicon body, which is formed perpendicularly to the plane of the wafer. The current flows parallelly to the wafer plane. The channel is wrapped by the gate electrodes in three directions. Figure 3 (a) and (b) illustrate the three-dimension structure and cross-section diagram of a FinFET device. FinFET can provide stronger control over the channel and suppress the SCEs, threshold current and gate-dielectric leakage current more effectively than MOSFET, resulting in higher on-state current, lower leakage and faster switching speed.

For better demonstration, the electrical characteristics of 32-nm FinFETs and 32-nm Bulk MOSFETs are investigated. The PTM is chosen as the model for the simulation due to the following reasons: PTM covers sufficient physical effects, and excellent scalability of PTM across process and design conditions have been shown in the published results. The primary parameters of the devices are listed in Table 1, which are typical of manufactured 32-nm FinFET and MOSFET.

Figure 4 illustrates the I-V characteristics of 32-nm n-type FinFET and Bulk MOSFET. The simulation results show that the FinFET achieves a higher $I_{\rm on}$ than MOSFET, which can provide higher drive strength. Moreover, owing to the strong gate control over the channel, the $I_{\rm off}$ of FinFET reduces significantly compared with MOSFET, demonstrating better suppression for the leakage current. Besides, it is distinct that the $I_{\rm DS}$ of FinFET climbs up sharply to the on-state level, while the ascending trend of NMOS is much slower. As a consequence of the difference, the FinFET can achieve a faster switching speed than bulk COMS, which makes FinFET applicable to high frequency application. On the other side, the faster switching times can also reduce the short-circuit power in the FinFET logic circuits.

Besides, the multi-gate structure provides more design flexibilities. It is worth noting that the front-gate and the back-gate of FinFET could be tied together or be controlled independently by different voltages, which provides three basic working modes for FinFET, namely Short-Gate mode, Independent-Gate mode and Low-Power mode.

I) Short-Gate (SG) mode, where the double gates are tied together, acting as a three-terminal device. The SG FinFET is a promising replacement for MOSFET. Higher on-state current and faster switch speed make it a high performance mode. And strong gate control offers better suppression for the SCEs and gate-dielectric leakage.

II) Independent-Gate (IG) mode, where the top part of the gate is removed to form two independent gates, acting as a four-terminal device. The front-gate and the back-gate can be connected to different inputs, and thus the IG FinFET can work as two parallel transistors, thus greatly reducing the number of transistors and improving the design flexibility.

III) Low-Power (LP) mode, where the back-gate is connected to a reverse-bias to reduce the threshold leakage. Actually it is a special case of IG mode. In this mode, the threshold leakage can be reduced by adjusting the back-gate voltage, expressed by

$$\frac{\partial V_{\rm th}}{\partial V_{\rm gb}} = -\frac{C_{\rm oxb}C_{\rm si}}{C_{\rm oxf}(C_{\rm oxb}+C_{\rm si})} \propto \frac{t_{\rm ox}}{t_{\rm si}}, \tag{1}$$

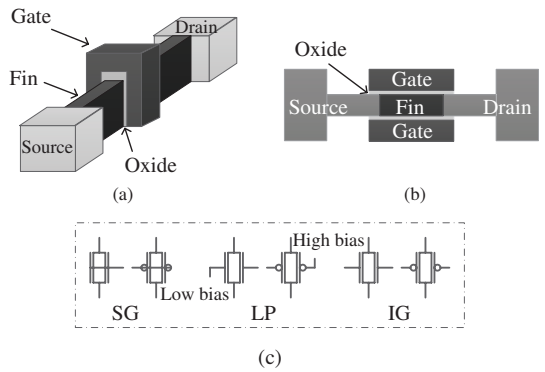

Figure 3 FinFET model and schematic. (a) Three-dimension structure; (b) cross-section diagram; (c) three working modes for FinFET.

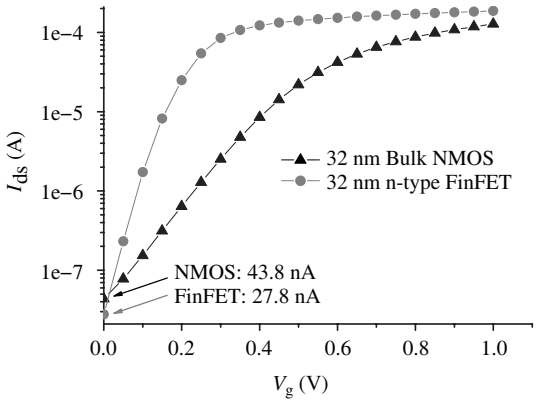

Figure 4 *I-V* characteristics of 32-nm n-type FinFET (W/L = 80 nm/32 nm) and 32-nm n-type MOSFET (W/L = 80 nm/32 nm).

Table 1 Primary parameters in PTM

Device		Primary parameters				
FinFET	n-type FinFET	$L_{\rm gate} = 32$ nm	$H_{\rm fin} = 40$ nm	$W_{\rm fin} = 8.6$ nm	$T_{\rm ox} = 1.4$ nm	$V_{\rm DD} = 1\,V$
	p-type FinFET	$L_{\rm gate} = 32$ nm	$H_{\rm fin} = 50$ nm	$W_{\rm fin} = 8.6$ nm	$T_{\rm ox} = 1.4$ nm	$V_{\rm DD} = 1\,V$
MOSFET	NMOS	$L_{\rm eff} = 32$ nm	$T_{\rm oxe} = 1.4$ nm	$V_{\rm DD} = 1\,V$	$V_{\rm th0} = 0.42\,V$	
	PMOS	$L_{\rm eff} = 32$ nm	$T_{\rm oxe} = 1.5$ nm	$V_{\rm DD} = 1\,V$	$V_{\rm th0} = -0.41\,V$	

in which the $C_{\rm si}$, $C_{\rm oxf}$, $C_{\rm oxb}$, $t_{\rm si}$ and $t_{\rm ox}$ are the body capacitance, front-gate capacitance, back-gate capacitance, fin thickness and oxide thickness, respectively. By (1), the threshold voltage of front-gate will be larger when the back-gate is tied to a reverse-bias. Since the leakage power is negatively correlated with the threshold voltage, the reverse-bias in back-gate could be used to control power consumption, especially leakage power.

Simulations are implemented to compare the different modes of FinFET operations. Figure 5 shows the variation in on-state and off-state currents across different modes of FinFET operations. The results indicate that the SG mode FinFET, which displays the highest $I_{\rm on}$, can provide the best drive strength. For IG mode FinFET, the drive strength declines obviously by about 50%. Compared with IG mode FinFET, application of reverse-bias in the LP mode FinFET further reduces the $I_{\rm on}$ at a small rate. For the off-state currents, the lowest $I_{\rm off}$ is achieved in LP mode FinFETs, which realizes a considerable $I_{\rm off}$ reduction compared to the SG and IG mode FinFETs.

However the coupling of the back-gate to front-gate is observed only in the weak inversion region of operation. In the region of strong inversion, the presence of inversion charge in the channel shields FinFET gates from each other and no coupling is observed. A generalized model for the relationship between the threshold voltage ($V_{\rm thgf}$) at the front gate (gf) of a FinFET and the voltage applied to its back gate (gb) is derived as follows [24]:

$$V_{\rm thgf} \approx \begin{cases} V^0_{\rm thgf} - \delta(V_{\rm gbs} - V_{\rm thgb}), & \text{if } V_{\rm gbs} < V_{\rm thgb}, \\ V^0_{\rm thgf}, & \text{other}, \end{cases} \tag{2}$$

where s denotes the source terminal of the FinFET, δ is a positive value determined by the ratio of gate and body capacitances, and $V^0_{\rm thgf}$ is the minimum observed $V_{\rm thgf}$. Eq. (2) is given for an n-type FinFET, but it may also be used for a p-type FinFET with the usual changes in sign.

$$t_{\rm pd} = \frac{k \cdot C_L \cdot V_{\rm dd}}{(V_{\rm dd} - V_{\rm TH})^{\alpha}}. \tag{3}$$

As is well known, threshold voltage increase will result in an exponential decrease of leakage power. But on the other hand, threshold voltage increase will result in the propagation delay increase as approximately

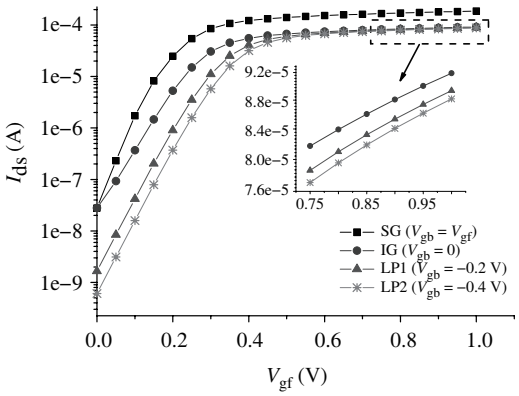

Figure 5 *I-V* characteristics of 32-nm n-type FinFET (W/L = 80 nm/32 nm).

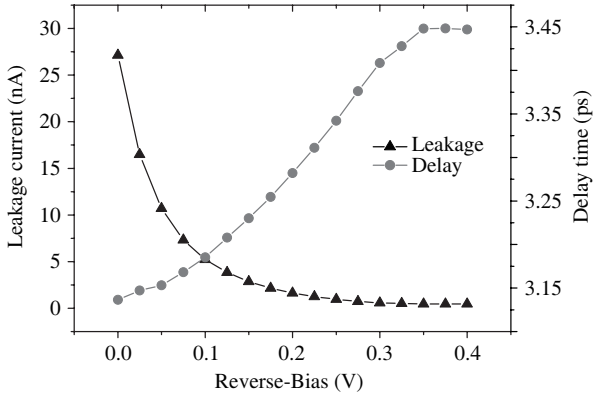

Figure 6 LP mode FinFET inverter delay and leakage variation (n-type FinFET: W/L = 80 nm/32 nm, p-type FinFET: W/L = 100 nm/32 nm).

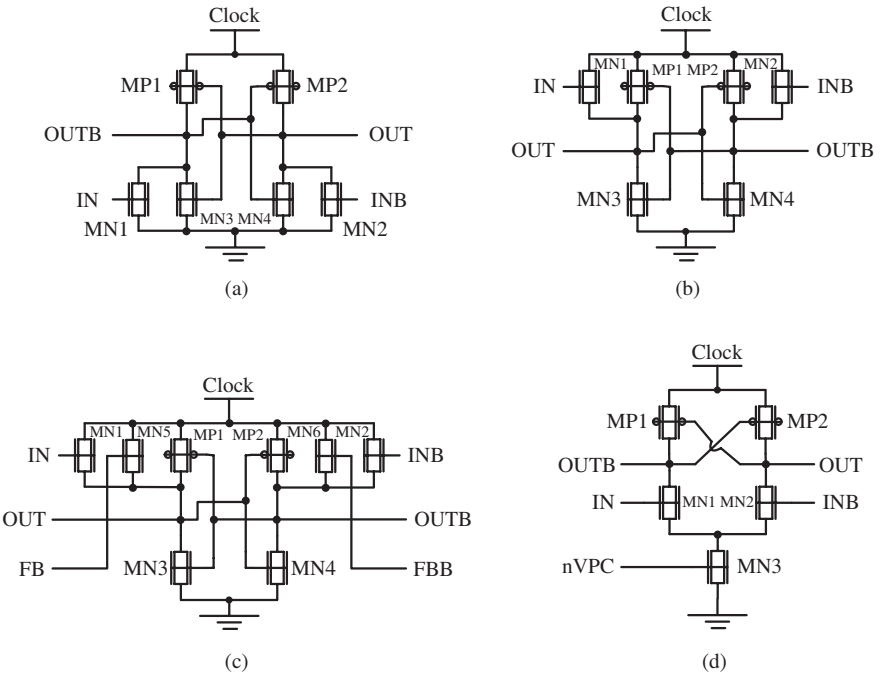

Figure 7 *I-V* characteristics of 32-nm n-type FinFET (W/L = 80 nm/32 nm) and 32-nm n-type MOSFET (W/L = 80 nm/32 nm). (a) 2N2N2P; (b) IPAL; (c) PFAL; (d) DCPAL.

given in (3), where α is typically 1.3 and k is a constant. Therefore it is necessary to find an appropriate reverse-bias to trade off the leakage and delay. An LP mode FinFET inverter of which both pull-up and pull-down were driven by a back-gate bias of equal strength was simulated as shown in Figure 6. Simulation results show that increasing the revers-bias will lead to an exponential decline in leakage current. Simultaneously the delay grows nearly linearly. It can be seen that the leakage curve displays an initial sharp decrease, but flattens out when reverse-bias exceeds 0.2 V. Further increasing the reverse-bias can only lead to delay overheads without much corresponding saving in leakage. Hence 0.2 V would be the most suitable value for the reverse-bias, which would be set as the reverse-bias in the following simulations.

Compared to MOSFETs, FinFETs demonstrate low-power characteristic, excellent performance and flexible working modes. Based on these advantages, our research successfully proposed some novel adiabatic logics based on FinFETs to further improve the power consumption and performance.

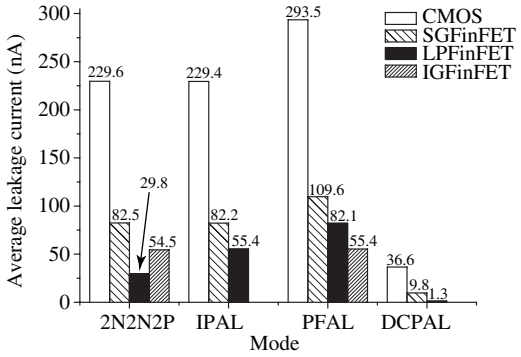

Figure 8 Average leakage current of different adiabatic buffers in the hold stage.

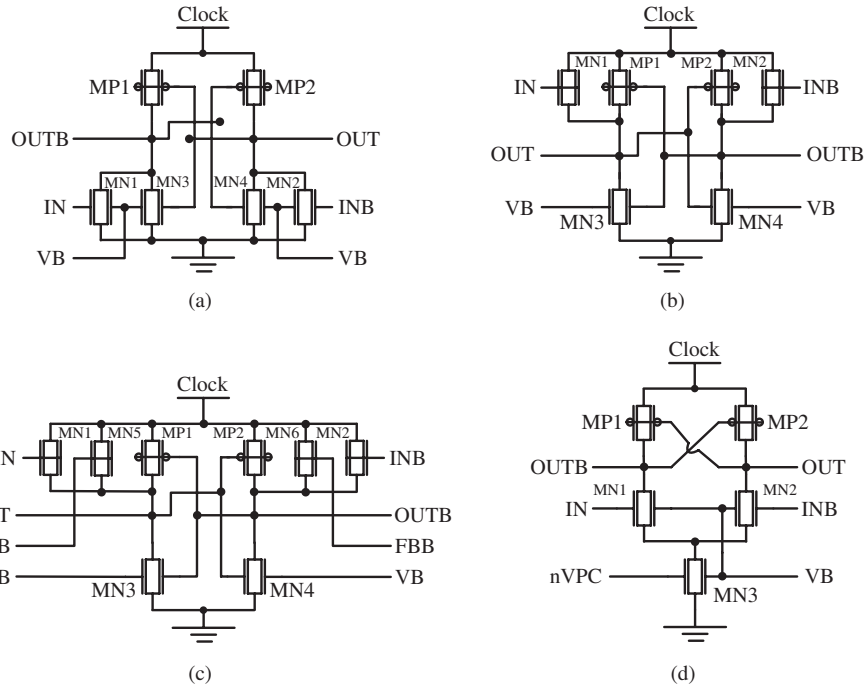

Figure 9 Four adiabatic buffer structures based on LP mode FinFET. (a) 2N2N2P; (b) IPAL; (c) PFAL; (d) DCPAL.

3 Proposed technique

Figure 7 illustrates four adiabatic buffer structures based on SG mode FinFETs. The SG mode FinFET circuit has lower off-state current and higher switching speed than MOSFET; thus it can effectively reduce the leakage current in every phase especially in the hold phase, and it greatly raises the limiting-frequency. Figure 8 compares simulation results of the average leakage current between the different mode FinFET adiabatic circuits and the MOSFET circuits in the hold phase. In the simulation, the minimum size FinFETs are simulated, that is, 80 nm/32 nm W/L ratio for n-type FinFET and 100 nm/32 nm ratio for p-type FinFET. The corresponding W/L ratio of MOSFET is 118 nm/32 nm for NMOS and 150 nm/32 nm for PMOS. The reverse-bias in the LP mode FinFET is set to 0.2 V. Results show that the leakage current of the SG mode FinFET adiabatic circuits are reduced by 64.1%, 64.2% and 62.7% respectively.

For the operation of adiabatic logic, the charging and discharging processes merely depend on the pull-up transistors, while the pull-down transistors primarily serve to accelerate the cross-coupling and maintain the certain nodes at zero voltage. Therefore the working speed of adiabatic circuits is determined by the pull-up transistors, independently of the pull-down parts. However the pull-down transistors have

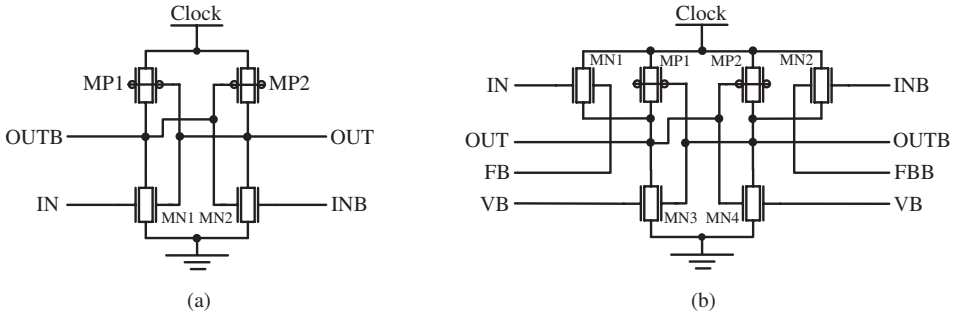

Figure 10 Structures of 2N2N2P and PFAL based on IG mode FinFETs. (a) 2N2N2P; (b) PFAL.

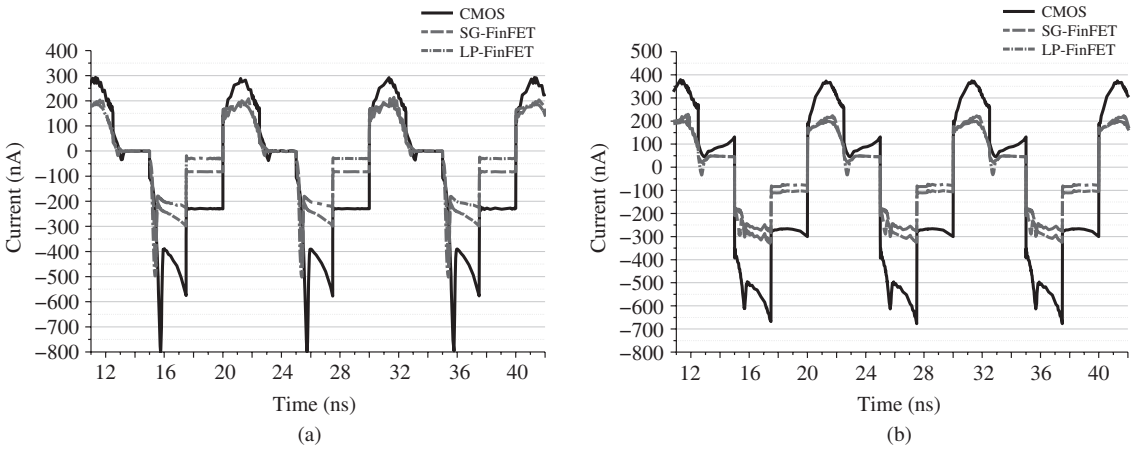

Figure 11 Current waveforms of (a) 2N2N2P adiabatic buffer and (b) IPAL adiabatic buffer.

great influences on the leakage current; it decides the power consumption. In order to further reduce the leakage power, we set the pull-down transistors in LP mode while keeping the pull-up transistors SG mode to maintain the circuit performance.

Figure 9 shows the four adiabatic buffers based on LP mode FinFET. The back-gates of pull-down transistors are connected to the reverse-bias to increase the threshold voltage. Thus most of the charge stored in the capacitance can flow back to the power supply instead of flowing to the ground in the recovery phase. Besides, choosing an appropriate reverse-bias is important, because excessive high reverse-bias would influence the speed while insufficient reverse-bias cannot provide efficient suppression for the leakage current. Through theoretical calculations and model simulation, the reverse-bias is set to -0.2 V, which is the best point to trade off the performance and power consumption. Figure 8 shows the LP mode FinFET adiabatic circuits' leakage current in hold phase. Compared with the MOSFET adiabatic circuits, the LP mode FinFET adiabatic circuits' leakage currents are reduced by 87.0%, 75.9%, 72.0% and 96.4% respectively, and moreover, they are 63.9%, 32.6%, 25.1% and 86.7% less than the SG mode FinFET adiabatic circuits.

Since the IG mode FinFET can work as two parallel transistors, certain adiabatic circuits that contain parallel transistors can be realized by IG mode FinFET to save power consumption and circuit area simultaneously. For example, the 2N2N2P adiabatic circuit contains two groups of parallel N-FinFETs in the pull-down paths, so these four transistors can be substituted by only two IG mode FinFETs. Results in Figure 8 show that the leakage current of IG mode 2N2N2P buffer is reduced by 54.5% compared with the SG mode one. The PFAL adiabatic buffer can also realize the IG mode structure, and the two groups of parallel N-FinFETs in the pull-up paths can be replaced by two IG mode FinFETs. Figure 10 gives the circuit structures of 2N2N2P and PFAL based on IG mode FinFETs.

For further demonstration, the adiabatic circuit's current waveforms based on different devices, namely MOSFET, SG mode FinFET and LP mode FinFET, are investigated. Figure 11 shows the results of the

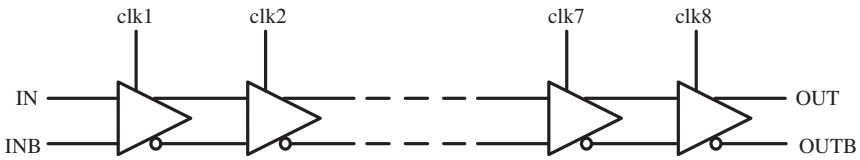

Figure 12 Structure of an 8-state clock chain.

2N2N2P adiabatic buffer and IPAL adiabatic buffer. The simulation frequency is set to 100 MHz and the time sequence is the same as in Figure 1. Detailed working processes of adiabatic circuits are presented in these waveforms. The negative current is the charging current which flow out from the power supply and the positive one represents the discharging current which flows back to the power supply. From the comparison, it is found that the reduction of power is significant after substituting FinFET for bulk CMOS.

Take 2N2N2P for example. Please note that the charging and discharging currents of MOSFET adiabatic buffer are about 500 nA and 300 nA, while the SG mode FinFET adiabatic buffer has a charging current of 250 nA and a discharging current of 200 nA. Obviously the energy recovering rate of FinFET adiabatic buffer is much superior to the MOSFET one. Additionally, leakage current is also an important issue to be considered. In the hold phase, the SG mode FinFET buffer's leakage current in the hold phase is about 80 nA, which is much lower than the MOSFET buffer that has a leakage current of about 220 nA. For the LP mode FinFET buffer, its energy recovering rate is as high as about 200 nA/ 210 nA; furthermore the leakage current, which is only 20 nA, is considerably low. Hence the LP mode FinFET adiabatic circuit is a good choice to realize the ultra-low-power design.

4 Simulation results

To demonstrate the effectiveness of our proposed adiabatic logic, simulations are conducted on an 8-state clock chain, based on the 32-nm PTM. Figure 12 illustrates the circuit's structure.

Here four adiabatic structures are investigated, namely 2N2N2P, IPAL, PFAL and DCPAL. In order to prove the advantages of FinFET adiabatic logic, these circuits are constructed by MOSFET, SG mode FinFET, LP mode FinFET and IG mode FinFET (for 2N2N2P and PFAL) respectively.

According to the operation of adiabatic circuits, eight-phase power clocks are set up and each clock is 90 degrees in advance of the previous one. Thus it consumes two clock periods to get the valid outputs after inputting the signals.

Simulations are performed on HSPICE using the 32-nm FinFET PTM and the 32-nm CMOS PTM. Since the power comparison between bulk CMOS adiabatic circuits and FinFET adiabatic circuits is based on the leakage current, for the accuracy of leakage comparison, the on-state current of bulk CMOS and FinFET are normalized to the same value by adjusting the W/L ratio of bulk MOSFET, which is to guarantee that the leakage currents are obtained from the circuits that have the same performance. Here the geometrical dimensions of FinFET and MOSFET, and the reverse-bias are set the same as the simulation in Section 3. In the simulation, a periodical input signal whose period is the same as the AC power supply is employed.

4.1 Power consumption

Since the clock chain is controlled by eight-phase clocks, we measured the average power dissipation of each clock and defined the sum of the eight clocks' average power as the total average power consumption. Figure 13 shows the results of our simulation. The longitudinal axis represents the average power consumption and the horizontal axis, whose value is logarithmic, stands for the clock frequency. The three curves in the coordinate system represent different transistors, i.e. SG mode FinFET, LP mode FinFET and MOSFET. For 2N2N2P and PFAL, the fourth curve represents the IG mode FinFET. In order to reflect the exhaustive information, the simulations are based on a range of frequency from 50 MHz to

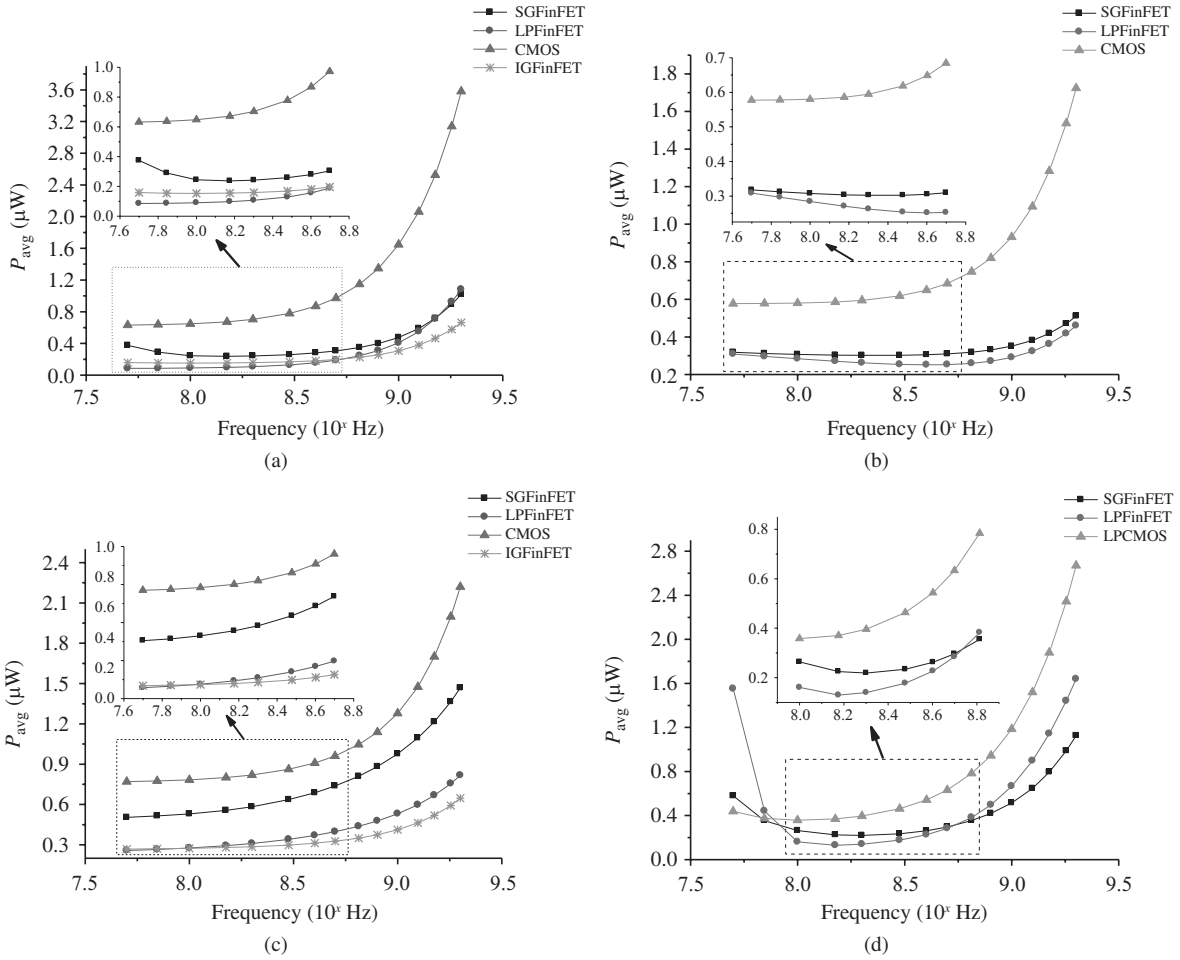

Figure 13 The average power of the four 8-state adiabatic clock chains. (a) 2N2N2P; (b) IPAL; (c) PFAL; (d) DCPAL.

Table 2 The average power of the four clock chains at 200 MHz

	CMOS (μW)	SG-FinFET (μW)	LP-FinFET (μW)	IG-FinFET (μW)
2N2N2P	0.70323	0.24234 (−65.5%)	0.10674 (−84.8%)	0.15845 (−77.5%)
IPAL	0.59468	0.30212 (−49.2%)	0.26234 (−55.9%)	
PFAL	0.81980	0.58305 (−28.9%)	0.30945 (−62.3%)	0.28542 (−65.2%)
DCPAL	0.39610	0.23432 (−40.8%)	0.17779 (−55.1%)	

2 GHz, which covers low-frequency, mid-frequency and high-frequency. Moreover, Tables 2 and 3 illustrate the detailed average power of the four type clock chains at 200 MHz and 2 GHz, which represent the mid-frequency and high-frequency respectively.

According to the simulation results, for all the adiabatic structures, i.e. 2N2N2P, IPAL, PFAL and DCPAL, the MOSFET clock chain consumes the most power and the LP or IG mode clock chain consumes the least. What is more, the reduction of power is outstanding after implementing the FinFET technology, especially for the LP mode FinFET clock chains, which coincides with the previous analysis. Moreover, it can be learned from Tables 2 and 3 that the improvement of power reduction becomes more significant as the frequency increases.

Analysis of the simulation results indicates that, for 2N2N2P clock chain, the power consumption based on MOSFET is much bigger than the IPAL and DCPAL clock chains, and it is similar to the PFAL's. However, by implementing the FinFET devices, the 2N2N2P clock chain realizes a tremendous power reduction and dissipates the least power at a wide range of frequency. For example, at 200 MHz frequency,

Table 3 The average power of the four clock chains at 2 GHz

	CMOS (μW)	SG-FinFET (μW)	LP-FinFET (μW)	IG-FinFET (μW)
2N2N2P	3.5802	1.0199 (−71.5%)	1.0820 (−69.8%)	0.66249 (−81.5%)
IPAL	1.7239	0.51043 (−70.4%)	0.46003 (−73.3%)	
PFAL	2.2191	1.4677 (−33.9%)	0.81699 (−63.2%)	0.64700 (−70.8%)
DCPAL	2.6696	1.1257 (−57.8%)	1.6411 (−38.5%)	

the power decreasing amplitudes of the SG, LP and IG mode FinFET clock chain reach 65.5%, 84.8% and 77.5% respectively compared to the MOSFET one, as can be seen in Table 2, and the values at 2 GHz achieve 71.5%, 69.8% and 81.5% respectively. This improvement is closely related to the buffer structure of 2N2N2P. According to Figure 3, the 2N2N2P's pull-down path, which is the access of leakage current, consists of four transistors, while the other structures only have two or three transistors. Based on the superiority on leakage suppression of FinFETs, accordingly the one which contains the most transistors in the pull-down path will have the best improved effect after replacing the MOSFET with FinFET. Additionally, the 2N2N2P logic needs the least transistors among the four adiabatic logics, which can effectively save the cost and area. It is predicted that the 2N2N2P logic based on FinFETs especially the IG mode FinFETs will be widely used in the future low-power design.

For the IPAL clock chain, the growth trend of its FinFET circuits' leakage power is much gentler than that of the others, which can be learned by comparing Figure 13. As a consequence, the FinFET IPAL clock chain consumes the least power at the high-frequency. For instance, at 1.5 GHz, the average power of SG mode FinFET IPAL clock chain is only 0.36 μW, which is much lower than that of the 2N2N2P (0.71 μW), PFAL (0.67 μW) and DCPAL (1.14 μW). Thus in the high-frequency application, the FinFET IPAL circuit is an ideal choice.

For PFAL, considerable power savings are also realized by the FinFETs. At 200 MHz, compared with CMOS adiabatic clock chain, the power reduction of SG mode FinFET clock chain is 28.9%, and the values of LP and IG mode clock chains even reach 62.3% and 65.2%. However, due to the complicated structure and its necessary feedback control loop, the power consumption of PFAL clock chain at mid-frequency is the largest no matter what the frequency is and what the mode is. The situation improves at high-frequency, at which the power reductions reach 33.9%, 63.2% and 70.8% for SG, LP and IG mode FinFET circuits respectively. However the power consumption is still not competitive compared with other structures. Therefore this structure is only adequate for some certain situations where complete recovery path and stable outputs are needed.

For DCPAL clock chain, its power consumption characteristic is really bad at low-frequency below 100 MHz. The power at low-frequency is much higher than that at mid-frequency, and moreover, the FinFET-based circuits' power even surpasses the bulk CMOS one. By investigating the DCPAL structure, it is concluded that the perverted phenomenon is owing to the severe coupling effect when the gating transistor is shut down. Please note that the power consumption would increase rapidly at high-frequency too. However, at mid-frequency (100 MHz–500 MHz), the power consumption is extremely low especially by applying the FinFET device. For example, at 200 MHz, the power is only 0.23 μW, which is the lowest among the four structures. Therefore DCPAL is a competing logic at mid-frequency.

It is worth noting that, for adiabatic clock chains based on IG mode FinFET, the power consumption is close to the LP mode FinFET clock chains and superior to the clock chains based on CMOS or SG mode FinFET. Moreover, the most attractive advantage of IG mode FinFET circuit is that it can greatly reduce the transistors in the circuits especially in the VLSI design which contains millions of transistors. Hence, ultra-low-power and considerable area saving make the IG mode FinFET adiabatic logic a promising structure to promote the IC design.

4.2 Limiting frequency

The realization of low power is usually at the expense of performance. Tremendous power reduction for adiabatic logic has been achieved by FinFET devices. Therefore it is necessary to investigate the

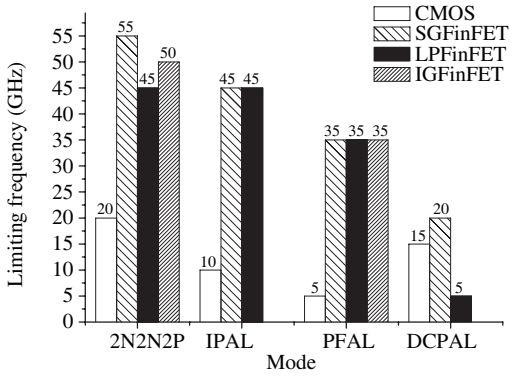

Figure 14 The limiting frequency of the four adiabatic clock chains.

performance of adiabatic circuits based on FinFETs. Here the limiting frequency is applied as the measure for performance. Continue increasing the frequency until the outputs become invalid, and then the stopping point is the limiting frequency. Figure 14 shows the limiting frequency of the four adiabatic clock chains based on different transistors.

Due to the higher on-state current and faster switching speed of FinFETs, it is observed from Figure 14 that the limiting frequency of FinFET adiabatic clock chain has a considerable improvement over the bulk CMOS circuit. Based on bulk CMOS, the limiting frequencies of 2N2N2P, IPAL, PFAL and DCPAL are 20 GHz, 10 GHz, 5 GHz and 15 GHz respectively. By substituting the SG mode FinFET, the value of 2N2N2P reaches as much as 55 GHz, which is the highest among the four clock chains, and the other three also realize tremendous increase of limiting frequency, i.e. 45 GHz for IPAL, 35 GHz for PFAL and 20 GHz for DCPAL. The LP mode FinFET is also successful for the test circuit. The LP mode 2N2N2P, IPAL and PFAL circuits' limiting frequency increase to 45 GHz, 45 GHz and 35 GHz respectively. Nevertheless, for DCPAL clock chain, the limiting frequency is only 5 GHz, which are even 10 GHz less than the bulk CMOS one. This irregular phenomenon is attributed to the more serious coupling effect after implementing the LP mode FinFET. For 2N2N2P and PFAL clock chains, significant improvements of limiting-frequency are also realized when they are based on the IG mode FinFET, i.e. 50 GHz for 2N2N2P and 35 GHz for PFAL.

To sum up, above comparison and discussion demonstrate that the use of low-power FinFET device does not sacrifice the performance. Instead it further improves the performance of the adiabatic circuit. It can be predicted that the improvement of leakage suppression and performance is also applicable to other FinFET adiabatic circuit structures. For further consideration, because the working speed of adiabatic circuits is determined by the pull-up paths and the pull-down paths have great influences on the leakage current, the W/L ratio of pull-up FinFETs can be increased to achieve a higher limiting frequency, while the pull-down FinFETs should be set to the minimum size to guarantee effective leakage suppression.

5 Conclusion

This paper presents the novel adiabatic logic based on FinFETs. Four types of adiabatic logic, namely 2N2N2P, IPAL, PFAL and DCPAL, are rebuilt by SG mode FinFET, LP mode FinFET and IG mode FinFET. Compared with the CMOS adiabatic logic, the proposed logic effectively reduces the power consumption and improves the performance. For further demonstration, simulations are performed on an 8-state adiabatic clock chain, based on 32-nm FinFET PTM and 32-nm CMOS PTM. Four kinds of transistors, i.e. MOSFET, SG mode FinFET, LP mode FinFET and IG mode FinFET, are investigated in the simulation. Simulation results show significant power savings by substituting FinFET with bulk CMOS, especially for LP mode FinFET which can realize ultra-low power design. For 2N2N2P, at 200 MHz, the power reduction of the SG, LP and IG mode FinFET clock chains reaches as high as 65.5%, 84.8% and 77.5% respectively, which achieves the greatest improvement among the four struc-

tures. And the improvement of power reduction becomes more significant as the frequency increases. Moreover, due to the higher on-state current and faster switching speed, the implementing of FinFET further improves the limiting frequency of adiabatic circuit. Besides considerable power reduction and performance improvement, it is worth noting that the IG mode FinFET can effectively reduce the transistors in the circuit, which contributes to great area saving in the VLSI design. Therefore, the low-power and high-performance FinFET adiabatic logic will be a competing structure in the future IC design.

References

1 Synopsys Inc. CCS Power Technical White Paper. Version 3.0, 2006
2 Denker J S. A review of adiabatic computing. In: IEEE Symposium on Low Power Electronics, San Diego, 1994. 94–97
3 Calhoun B H, Khanna S, Mann R, et al. Sub-threshold circuit design with shrinking CMOS devices. In: IEEE International Symposium on Circuits and Systems, Taipei, 2009. 2541–2544
4 Hemantha S, Dhawan A, Haranath K. Multi-threshold CMOS design for low power digital circuits. In: 2008 IEEE Region 10 Conference on TENCON, Hyderabad, 2008. 1–5
5 Li L F, Hu J P, Yu L L. Low-power register file using N-type and P-type adiabatic logic circuits. In: Pacific-Asia Conference on Circuits, Communications and Systems, Chengdu, 2009. 342–345
6 Samson M, Mandavalli S. Adiabatic 5T SRAM. In: 2011 International Symposium on Electronic System Design, Kochi, 2011. 267–272
7 Chanda M, Dandapat A, Rahaman H. Low-power sequential circuit using single phase adiabatic dynamic logic. In: 2009 International Conference on Computers and Devices for Communication, Kolkata, 2009. 1–4
8 Bai X F, Huang L, Wang Y F, et al. Evaluation of DPA attack resistance of transistor-based adiabatic logic styles. In: 2nd International Conference on e-Business and Information System Security, Wuhan, 2010. 1–3
9 Monteiro C, Takahashi Y, Sekine T. Resistance against power analysis attacks on adiabatic dynamic and adiabatic differential logics for smart card. In: International Symposium on Intelligent Signal Processing and Communications Systems, Chiang Mai, 2011. 1–5
10 Mukhopadhyay S, Raychowdhury A, Roy K. Accurate estimation of total leakage in nanometer-scale bulk CMOS circuit based on device geometry and doping profile. IEEE Trans Comput Aid Des Integr Circuit Syst, 2005, 24: 363–381
11 Hisamoto D, Lee W C, Kedzierski J, et al. FinFETA self-aligned double gate MOSFET scalable to 20 nm. IEEE Trans Electron Dev, 2000, 47: 2320–2325
12 Thakker R A, Sathe C, Sachid A B, et al. A novel table-based approach for design of FinFET circuits. IEEE Trans Comput Aid Des Integr Circuit Syst, 2009, 28: 1061–1070
13 Endo K, O'uchi S I, Ishikawa Y, et al. Independent-double-gate FinFET SRAM for leakage current reduction. IEEE electron dev lett, 2009, 30: 757–759
14 Hsieh C Y, Fan M L, Hu V P H, et al. Independently-controlled-gate FinFET Schmitt trigger sub-threshold SRAMs. IEEE Trans Very Large Scale Integr Syst, 2012, 20: 1201–1210
15 Jafari F, Mosaffa M, Mohammadi S. Designing robust asynchronous circuits based on FinFET technology. In: 2011 14th Euromicro Conference on Digital System Design, Oulu, 2011. 401–408
16 Rasouli S H, Koike H, Banerjee K. High-speed low-power FinFET based domino logic. In: Asia and South Pacific Design Automation Conference, Yokohama, 2009. 829–834
17 Mishra P, Muttreja A, Jha, N K. Evaluation of multiple supply and threshold voltages for low-power FinFET circuit synthesis. In: IEEE International Symposium on Nanoscale Architectures, Anaheim, 2008. 77–84
18 Kramer A, Denker J S, Flower B, et al. 2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits. In: Proceedings of the 1995 International Symposium on Low Power Design. New York: ACM, 1995. 191–196
19 Varga L, Kovacs F, Hosszu G. An improved pass-gate adiabatic logic. In: 14th Annual IEEE International ASIC/SOC Conference, Arlington, 2001. 208–211
20 Blotti A, Saletti R. Ultralow-power adiabatic circuit semi-custom design. IEEE Trans Very Large Scale Integr Syst, 2011, 12: 1248–1253
21 Bhaaskaran V S K. Energy recovery performance of quasi-adiabatic circuits using lower technology nodes. In: 2010 India International Conference on Power Electronics, New Delhi, 2011. 1–7
22 Zhao W, Cao Y. Predictive technology model for nano-CMOS design exploration. ACM J Emerg Technol Comput Syst, 2007, 3: 1
23 Moon Y, Jeong D K. An efficient charge recovery logic circuit. IEEE J Solid-State Circuits, 1996, 31: 514–522
24 Trivedi V P, Fossum J G, Zhang W M. Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra-thin bodies. Solid-State Electron, 2007, 1: 170–178