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• BRIEF REPORT •

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A 65 mW fully integrated UHF-band CMMB tuner in 65 nm CMOS process

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Abstract A low power fully integrated digital TV tuner chip for China Mobile Multimedia Broadcasting (CMMB) application is presented. Based on direction conversion architecture, analog 8th-order filter/gain stages utilizing high power efficient operation-amplifiers and a $\Sigma\Delta$ fractional-N phase locked loop (PLL) with one voltage controlled oscillator (VCO) covering 4.8—7.2 GHz is proposed for low power and small chip area. The tuner is implemented in 65 nm CMOS process with low noise amplifier (LNA) matching network and phase locked loop (PLL) filter integrated on chip, occupying a chip area of 4.83 mm^2. The measured noise figure (NF) is less than 3.2 dB over CMMB UHF band (470—798 MHz). A total power consumption of 65 mW (54 mA from 1.2 V supply) is achieved.

Keywords CMMB, digital TV, tuner, receiver

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1 Introduction

The China Mobile Multimedia Broadcasting (CMMB) is China's mobile TV standard based on Satellite-Terrestrial Interactive Multi-service Infrastructure [1]. Since the commercialization of CMMB in 2008, satellites and terrestrial base stations have been continuously set up, while high performance RF tuner is still in need. Firstly, the power consumption of the tuner will directly affect active time of the TV terminal with limited battery. According to the CMMB standard, the mobile TV terminal should sustain 3 hours' of TV active time [1]. However, this requirement is far less than actual demand. Secondly, as CMMB tuner is usually one part of a smart handset, a highly integrated tuner chip is desired for low cost and large scale application. In this work, both power consumption and integration are optimized, and a fully integrated RF tuner is implemented in 65nm CMOS process with power consumption of 65 mW.

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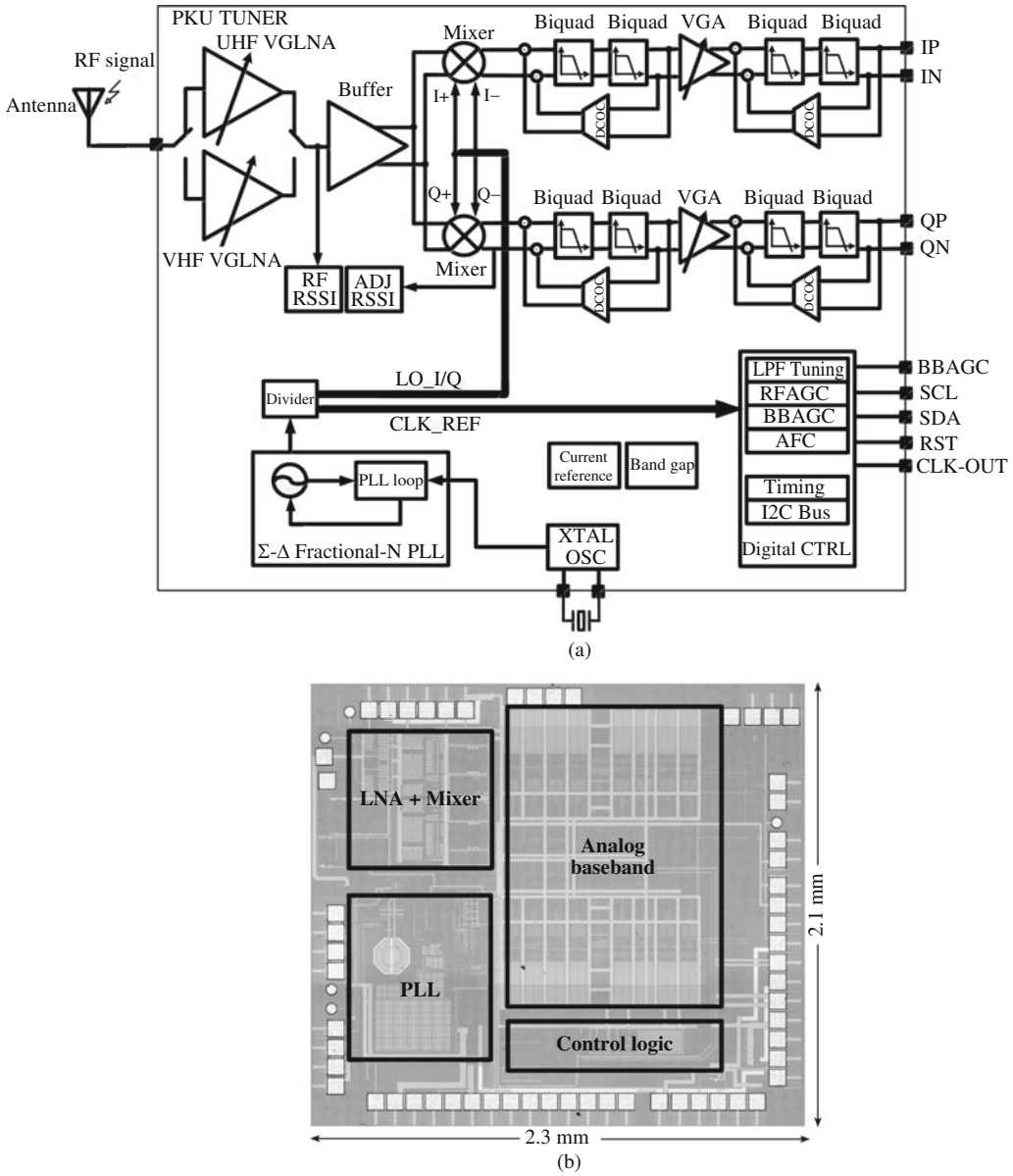

Figure 1 Proposed CMMB tuner system (a) and chip microphotograph (b).

2 System architecture and design consideration

The proposed tuner system with direct-conversion architecture is shown in Figure 1(a). Compared with low IF architecture, direct-conversion receiver needs no image rejection and the analog base-band works under half of the signal bandwidth; therefore the power for intermediate frequency (IF) and baseband can be reduced. In Figure 1(a), the single-ended input from antenna is amplified by a variable-gain low noise amplifier (VGLNA) and converted into differential signals for passive mixers. The following analog baseband circuits realize baseband signal filtering with variable gain before output I/Q analog signals (IP, IN, QP and QN). A fractional-N phase locked loop (PLL) is adopted to generate quadrature local oscillation (LO) signals for I/Q mixers. The maximum gain of the receiver link is 110 dB, including 27 dB LNA gain, 18 dB mixer gain and 70 dB analog baseband gain. The gain controlling is realized with RF RSSI, ADJ RSSI, digital baseband feedback control and an optimized lookup table.

LNA plays an important role in balancing NF and linearity of CMMB tuner as the tuner is required

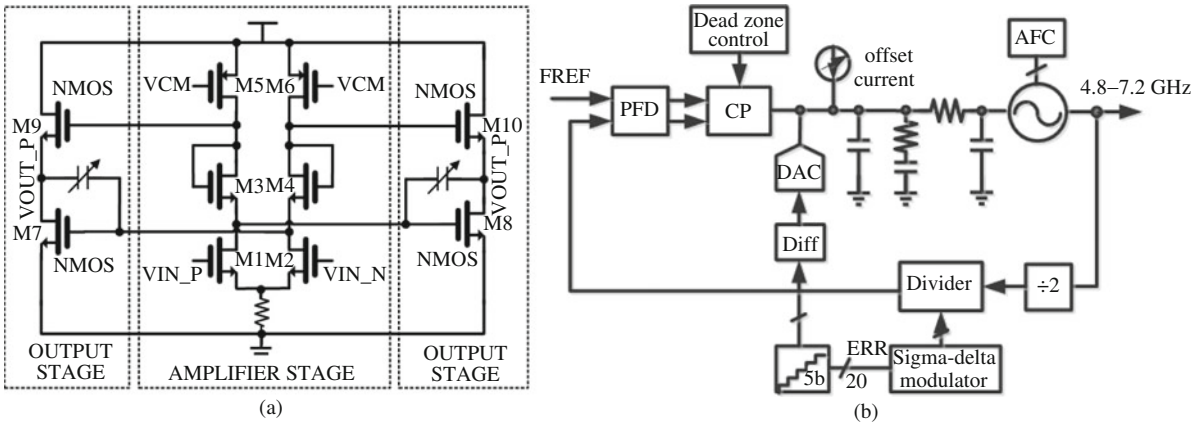

Figure 2 High power efficient operational amplifier (a) and fractional-N PLL (b).

to work under a large dynamic range of RF signals and high interference from adjacent channels. In order to achieve low power and low NF, an LNA with noise cancelling structure [2] is adopted for NF of about 2 dB. A gain range from −30—27 dB is realized to meet the requirement of large input dynamic range. The positive gain adjusting is realized with load resistor network, and the negative gain is achieved by passive attenuation network. Passive mixers are used to realize high linearity and low flick noise corner. Between the LNA and the mixers, a buffer stage is inserted to balance the output impedance seen by the mixers.

Analog baseband usually consume much power for high out-of-band rejection and high gain. In this work, four active filter biquads with positive gain are cascaded to realize an 8th order Chebyshev low pass filter with gain up to 70 dB. Since operational amplifiers are shared for filtering and amplifying, the power consumption is nearly halved. Moreover, a highly efficient operation amplifier similar to that of [3] is proposed to further decrease the analog baseband power consumption. In this two-stage operation amplifier, as shown in Figure 2(a), the first stage realize high gain/power ratio with push-pull structure, and the second stage with a zero cancels the pole of the first stage to extend the bandwidth without additional power penalty. As 8th order filtering and up to 70 dB gain are required for baseband, dc-offset could be significant; therefore two DCOCs in each I/Q branch are used. In the DCOC loop, high pass corner switching technique [4] helps to realize 20 μs settling time and 12 kHz corner.

The LO is required to cover a large frequency range (470—798 MHz), but it is difficult to achieve such tuning range with a single VCO. At the same time, LC VCO oscillating under 1 GHz usually consumes much power and chip area. In this work, a VCO work at 8X frequency (4.8—7.2 GHz) is designed to alleviate this problem. With the help of the dual-modulus divider (divide by 2/3), a continuous frequency range of 1.6–3.6 GHz is achieved, after two divide-by-2's, 400—900 MHz I/Q LO signals are obtained. As a result, the power consumption and chip area for frequency generation are both optimized. The LC VCO is composed of cross-coupled PMOS pair for negative impedance, and a tail resistor network to adjust the oscillating amplitude for optimized phase noise. A fractional-N PLL with third-order ΣΔ modulator is adopted for fine frequency steps as shown in Figure 2(b), and noise compensation techniques are adopted to suppress impact from nonlinearity and mismatches. A lead-lag passive loop filter is implemented on chip, and stacked MOS capacitor and MIM capacitor are used to shrink the filter's chip area.

3 Experiment results

The proposed tuner is fabricated in 65 nm CMOS process with a chip area of 4.83 mm^2, as shown in Figure 1(b). The tuner chip is measured under UHF band, as shown in Figure 3(a), and the system gain and NF are 88—90 dB and 2.0—3.6 dB, respectively. The phase noise is tested to be −115 dBc/Hz@1 MHz for 5.462 GHz. QPSK and 16QAM signals are also tested and clear constellation is obtained, as shown in Figure 3(b). Under QPSK mode (1/2code rate),sensitivity of −95 dBm is achieved. The power consump-

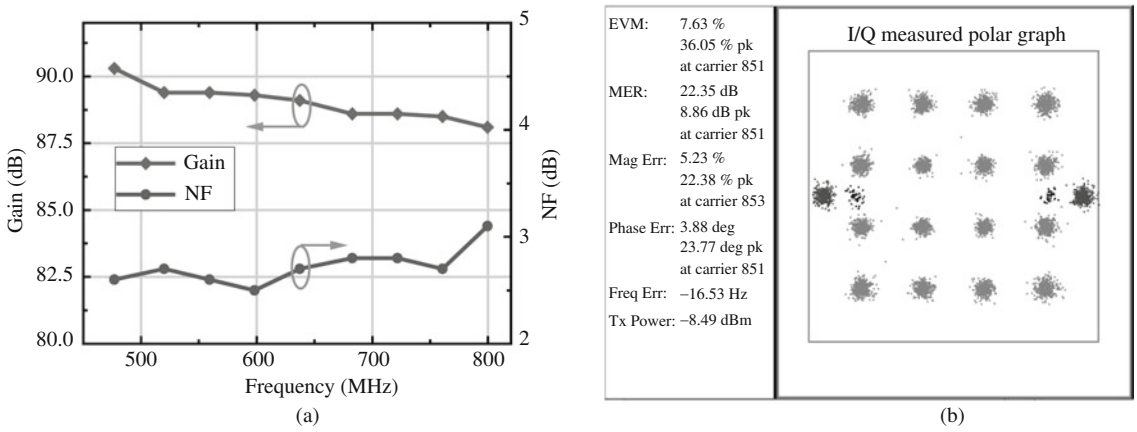

Figure 3 Measured system gain and NF (a), and 16QAM constellation (b).

Table 1 Performance summary and comparison

Ref. -Year	[5] RFIC, 2010	[6] ISSCC 2009	[7] JSSC, 2009	This Work
Technology	65 nm CMOS	130 nm CMOS	130 nm CMOS	65 nm CMOS
Power(mW)	100	67	114	65
Vdd(V)	1.8/1.2	1.2	1.2	1.2
Die Size(mm^2)	6	4	7.2	4.83
Operation Band	VHF/UHF	UHF	UHF/L	UHF
NF(UHF)	3.5—4.8	3.0	3.7—4.3	2.5—3.1
Max input (dBm)	NA	+10	−15	−10
IIP3(dBm)	NA	+20@max. attenu.	+5 @ −15 dB	14.7 @−16 dBm
IIP2(dBm)	NA	NA	+50 @ −15 dB	48.2 @−16 dBm
Filter Rejection @5.25 MHz	NA	48 dB	32 dB	48 dB

tion for the front-end, the baseband and the PLL are 12, 20 and 15 mA, respectively, and the total current is 54 mA, corresponding to 65 mW. This power consumption is less than that of recently reported state-of-the-art UHF tuners as shown in Table 1. The chip is also tested in a smart phone taking place of a commercial tuner chip, and fluent CMMB TV program is played.

4 Conclusions

A CMMB tuner for UHF band is presented in this paper. The system architecture and circuit blocks are optimized for low power operation. Fabricated in 65 nm CMOS process, the proposed chip achieves a total power consumption of 65 mW, which is lower than that of recent reported UHF tuners. As matching network and PLL filter are realized on chip, high integration is also realized.

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