A low-jitter low-power monolithically integrated optical receiver for SDH STM-16

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Abstract   A high-scale integrated optical receiver including a preamplifier, a limiting amplifier, a clock and data recovery (CDR) block, and a 1:4 demultiplexer (DEMUX) has been realized in a 0.25 μm CMOS technology. Using the loop parameter optimization method and the low-jitter circuit design technique, the rms and peak-to-peak jitter of the recovered 625 MHz clock are 9.4 and 46.3 ps, respectively, which meet the jitter specifications stipulated in ITU-T recommendation G.958. In response to 2.5 Gb/s PRBS input data ($2^{23}-1$), the recovered and frequency divided 625 MHz clock has a phase noise of -83.8 dBc/Hz at 20 kHz offset and the 2.5 Gb/s PRBS data has been demultiplexed into four 625 Mb/s data. The power dissipation is only 0.3 W under a single 3.3 V supply (excluding output buffers).

1 Introduction

Optical communication systems, which are used in backbone networks or wide area networks (WANs), are expected to play an important role in realizing the future multimedia society. These systems must be compact, economical to produce, and efficient in terms of power consumption. Given these requirements, researchers have been developing small-size and low-power optical receiver (OR) modules for the regenerators and line terminals of systems such as SDH or SONET.

The CDR is one of the key components of an OR, which must have retiming, reshape and regeneration (3R) operation [1, 2]. A phase-locked loop (PLL) is a preferable approach to develop a CDR, in which the phase of the clock in the decision circuit is automatically synchronized to the center of each bit. Also, the PLL can be integrated into a single integrated circuit (IC), greatly reducing temperature drift and phase relationship problems.

A number of optical receiver ICs integrated with preamplifier, limiter, clock and data recovery (CDR), and demultiplexer (DEMUX) have been realized [3–5]. However, they generally require large chip area and provide poor jitter characteristics due to the integration of different function blocks in the IC.

This paper advances a method of designing Charge Pump Phase-Locked Loops (CPPLL), in which the phase detector can detect the phase in generating early-late phase logic and its special function is to demultiplex the data acting as a 1:2 demultiplexer. Therefore, the three blocks containing clock recovery, data decision and 1:4 demultiplexer are integrated monolithically.

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2   Low-jitter design technique

The jitter transfer function of the CDR, which shows the input jitter suppression characteristics, can be expressed by substituting the phase-transfer function for the jitter transfer function:

$$H(j\omega) = \frac{\omega_n^2 + j(2\xi\omega_n - \frac{\omega_n^2}{K})\omega}{\omega_n^2 - \omega^2 + j2\xi\omega_n\omega}. \tag{1}$$

When the loop-filter is a lag-lead type (the series and shunt resister are R_1 and R_2 respectively and the shunt capacitance is C), the natural angular frequency ω_n and the damping factor ξ are expressed as

$$\omega_n = \sqrt{\frac{K}{\tau_1 + \tau_2}}, \quad \xi = \frac{1}{2}\omega_n\left(\tau_2 + \frac{1}{K}\right), \tag{2}$$

where $\tau_1 = C(R_1 + R_2)$ and $\tau_2 = CR_2$. $\xi\omega_n$ can be expressed as a constant Z_W. To meet the jitter transfer specification for STM-16 stipulated in ITU-T recommendation G.958, Z_W has to be lower than 6 MHz.

Once Z_W and the lower limit of ξ are fixed and $\tau_2 \gg 1/K$, the lower limit of τ_2, which is one of the loop filter time constants, is also fixed by (3):

$$\tau_2 = 2\xi^2/Z_W. \tag{3}$$

Also the pull-in range can be expressed as (see [6])

$$\Omega_p = 2Z_W\sqrt{2\left(\frac{\tau_1}{\tau_2} + 1\right)}. \tag{4}$$

It is recommended that the jitter peaking be lower than 0.1 dB, which fixes the lower limit of ξ at $\xi > 4$. The open loop gain K which includes the product of phase detector sensitivity K_{PD}, VCO modulation factor K_{VCO} and so on, is limited in the circuit design. Thus τ_1 can be inferred from eq. (2).

3   Receiver architecture

The architecture of the optical receiver is shown in Figure 1, and the incoming optical signal is first converted into electrical pulses by the photo diode. A preamplifier and a limiting amplifier are implemented to improve the input sensitivity, and then the 2.5 Gb/s input data is introduced to the four parallel latch chains generating the six samples. The sampling circuit acts as phase detector and 1:2 demultiplexer simultaneously. This half-bit-rate architecture of the CDR/DEMUX IC is based on the concept reported in [7] and has already realized in our previous work [8]. The combination of the PD and the 1:2 DEMUX adopts a 1.25 GHz half-bit-rate clock provided by VCO.

Additionally, the early-late phase logic circuit consists of four XORs and two selectors. It detects whether the clock with respect to the incoming data transition is early or late. It has simpler logic and less transistor than those of other work [2]. This early-late phase logic circuit provides the Early-Late control signal for the charge pump.

To convert the two 1:2 demultiplexed 1.25 Gb/s signals a2, and c2 into commercially available 625 Mb/s DEMUX ICs, an additional 2:4 demultiplexer is included, which produces four 625 Mb/s output signals D0, D1, D2, D3, and the 625 MHz output clock Clk.

4   Building blocks

4.1   Preamplifier and limiting amplifier

A preamplifier and a limiting amplifier constitute the front-end circuit of the optical receiver. The preamplifier converts the small current pulse signal from the photo diode to a certain voltage pulse signal and it must have low noise characteristic as the input signal is faint. The preamplifier must provide a high enough gain to acquire high sensitivity and low bit error rate (BER). On the other hand, it should
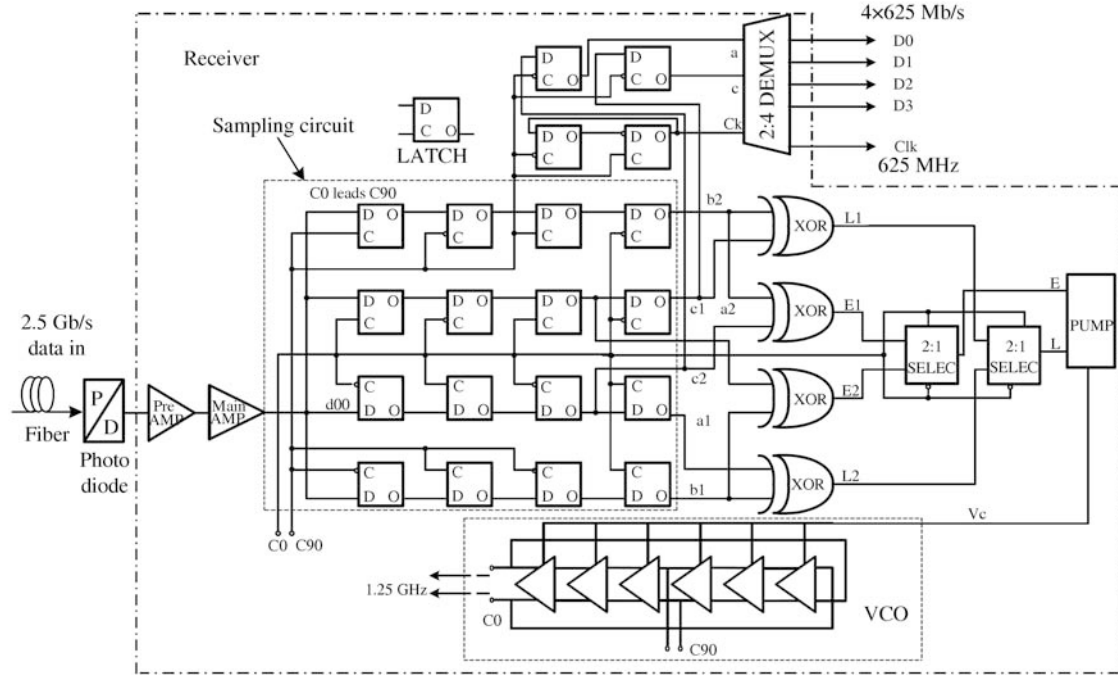
Figure 1 Receiver architecture.

have appropriate bandwidth to enable the receiver to operate at given speed level and correspond to a small noise. In engineering application, the bandwidth is chosen at 0.8 times of the data rate. The elementary trans-impedance preamplifier structure is shown in Figure 2. The feedback resistor R_f provides voltage shunt negative feedback and it converts current into voltage.

The preamplifier cannot attain high enough gain on the condition of low noise and appropriate bandwidth, and the signal should be amplified further to obtain required amplitude. The limiting amplifier converts the output signal into a high enough and invariable output voltage to drive the later clock recovery and data decision circuit. The limiting amplifier contains five broad-band amplifiers to obtain large enough dynamic range. An effective way to increase the bandwidth is to introduce an inductive component into the loads of each gain stage. The cell of the limiting amplifier with active inductor loads is illustrated in Figure 3. According to the small-signal model of an active inductor, its equivalent input impedance can be written as

$$Z_{\text{in}} = \frac{1 + R_g s C_{gs}}{g_m + s C_{gs}}. \tag{5}$$

Thus, the equivalent inductance L and serial resistance R can be obtained from eq. (5). The bandwidth of the maximum flatness gain can be about 1.72 times as large as that of the same stage without inductor compensation.

4.2 VCO and charge pump

VCO adopts six stages ring oscillators and produces two clock signals C0 and C90 with a 90 degree phase shift, as shown in Figure 1. The control of the VCO is split into a coarse input and a fine input. The fine control is established by the phase detector and the coarse control is a provision for the change of temperature and technology. Figure 4 shows the delay cell of the VCO, which has a differential structure in order to reduce the power-supply-injected phase noise.

Figure 5 describes the schematic of the differential charge pump where differential pairs M1-M2 and M3-M4 are driven by the early-late phase logic circuit. The Early and Late signals activate only pull-down currents, and the pull-up currents are passive. Thus, when both Early and Late are low, a common-mode feedback circuit must counteract the pull-up currents to maintain a proper level. The feedback network
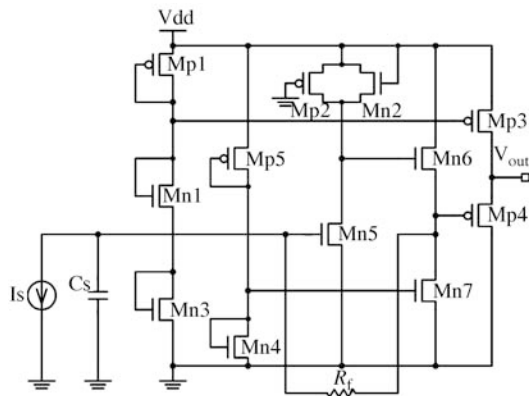
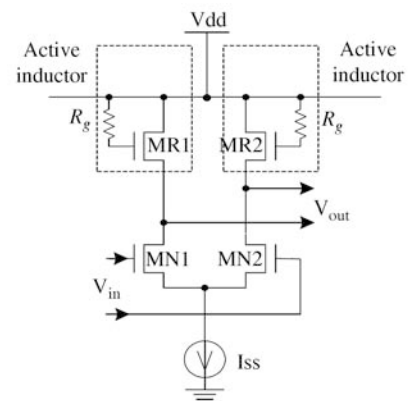**Figure 2**   Transimpedance preamplifier.

Figure 3   Broad-band amplifier with active inductor loads.
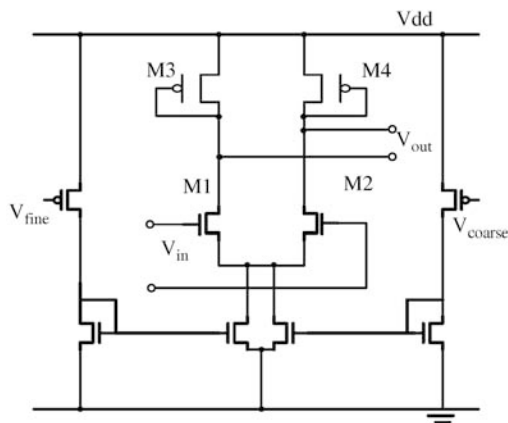

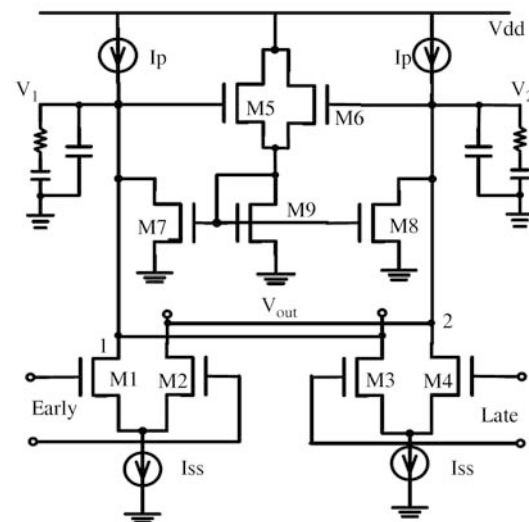**Figure 4**   Delay cell of the six stages ring oscillators.

Figure 5   Schematic of differential charge pump.

consisting of M5-M9 sets the output common mode level at $V_{GS5}+V_{GS9}$. An additional advantage is that the differential implementation alleviates the mismatch and charge-sharing problems [9].

4.3   Low-jitter design procedure

Loop parameter optimization scheme is implemented to achieve low jitter performance, and the parameters of the loop filter are specified in accordance with eqs. (2)–(4). Furthermore, the capacitor C of the loop filter can be decreased to so a small a value as to be integrated in chip by reducing the open loop gain K as from eq. (2). The whole receiver chip has no external components and is highly integrated. The loop parameter optimization can comply with this flow to suppress jitter and obtain compacted architecture.

In addition to achieving jitter reduction through the loop parameter optimization, noise generation in the noise sources and noise leakage between circuits in the IC must be reduced as much as possible. The method of differential circuits is adopted to reduce the disturbing common-mode noise and the jitter generation of the IC. To reduce the noise leakage, the function areas of the chip are separated as far as possible from each other and substrate contacts are inserted in between them [10].
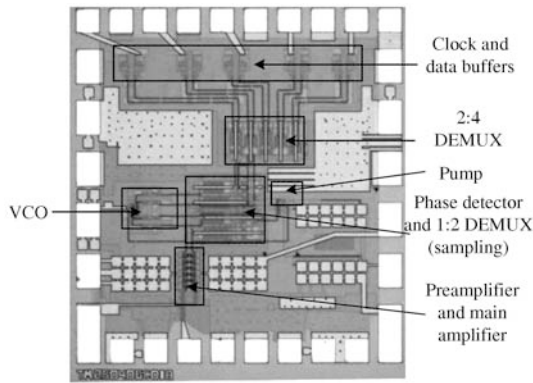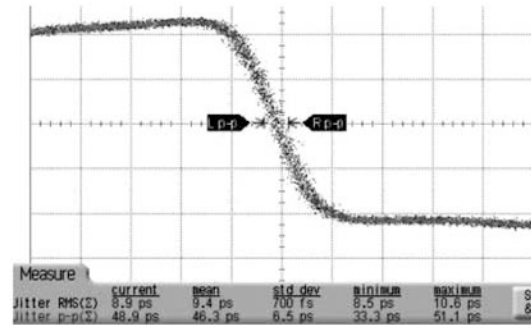
Figure 6 Chip micrograph of the receiver.

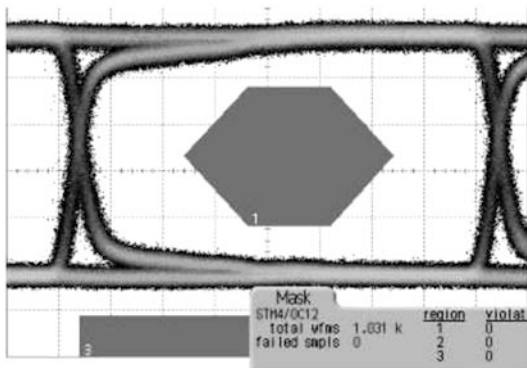**Figure 7** The jitter of the recovered 625 MHz clock.

Figure 8 Eye diagram of the output data and STM4/OC12 mask.
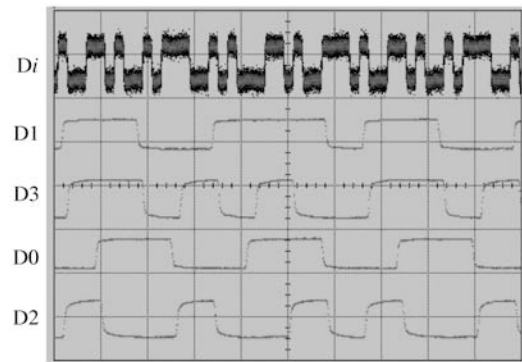

Figure 9 The waveforms with one 2.5 Gb/s input and four 625 Mb/s output data.

5 Experimental results

The 2.5 Gb/s optical receiver IC is realized in TSMC standard 0.25 μm single-poly 5-metal (5M1P) CMOS technology via the multi-project wafer (MPW) service of our institute. The cutoff frequency f_T of this process is about 18 GHz. A micrograph of the fabricated chip is shown in Figure 6. The chip size, including the bonding pads, is only 0.97 mm × 0.97 mm, and its power dissipation is 650 mW with a single 3.3 V power supply.

The performance of the fabricated receiver IC is measured on-wafer together using a pulse pattern generator (Advantest D3186), a broad bandwidth oscillograph (Agilent DCA 86100A), a cascade probe station and 40 GHz microwave probes. The recovered 625 MHz clock spectrum with a 9 mV 2.5 Gb/s $2^{23}-1$ pseudorandom bit sequences (PRBS) input data exhibits a phase noise of -83.8 dBc/Hz at 20 kHz off the center frequency. Figure 7 shows that the measured rms and peak-to-peak jitter of the 625 MHz clock are 9.4 and 46.3 ps, corresponding to 0.0059 and 0.029 UI, respectively. It meets the jitter specifications of the ITU-T recommendation G.958 which stipulates the rms, and peak-to-peak jitters are lower than 0.01 and 0.1 UI, respectively.

An eye diagram of the well regenerated and demultiplexed 625 Mb/s data signal of the output D0–D3 is shown in Figure 8. It indicates that the eye opening of the output data was sufficiently wide and free of the chip functions error while contrasting the eye diagram with STM4/OC12 mask.

Figure 9 shows the waveforms of one 2.5 Gb/s input datum and four pieces of 625 Mb/s output data, where Di is the input data and D0, D1, D2, and D3 are the output data. It is shown that one serial datum has been correctly demultiplexed into four parallel lower speed data.

The amplitude of the input data Di in Figure 9 is 8 mV, or even smaller, as the minimum amplitude is limited by the 2 mV noise floor of the source generator (Advantest D3186). Corresponding to 8 mV input voltage, the input current is 20 μA. Thus the actual input sensitivity of the receiver should be less

Table 1 Comparison of performance with other work

	This work	Ref. [11]	Ref. [12]	Ref. [13]
Process	0.25 μm CMOS	0.5 um Si-bipolar	0.7 um Si-bipolar	0.35 μm CMOS
	(f_T=18.6 GHz)	(f_T=40 GHz)	(f_T=27 GHz)	(f_T=14 GHz)
Power supply	650 mW	1.1 W	500 mW	100 mW
Core supply	300 mW	680 mW	350 mW (no demux)	100 mW
Supply voltage	+3.3 V	+3.3 V	+3.3 V	+3 V
Area	0.97 mm × 0.97 mm	3 mm × 5 mm	2 mm × 2 mm	1.65 mm × 1.5 mm
Gate count	800	400	350	150
Functions	PreAmp+Limited	Limited Amp+	Limited Amp+	PreAmp+
	Amp+CDR+1:4DEMUX	CDR+1:8DEMUX	CDR	Limited Amp
Clock RMS jitter	0.0059 UI	0.008 UI	0.025 UI	0.12 UI

than 20 μA. This is due to the fact that the sensitivity is limited by the SNR of the input signal.

The receiver exhibits a pull-in range of 80 MHz, and the tuning range of the VCO coarse control is 400 MHz, covering the frequency deviation caused by fluctuations in technology, temperature and voltage. In addition to a low jitter, this receiver achieves a small chip area and power that is substantially lower than that of other designs. The comparison list in Table 1 shows that the primary performance of this work is superior to previous research [11–14].

6 Conclusions

A complex (∼800 transistors and 1 mm square) mixed-signal receiver chip with on-chip preamplifier, limiting amplifier, clock and data recovery, and 1:4 demultiplexer was successfully realized in a standard 0.25 μm CMOS technology. The half-rate phase detector provides a bang-bang characteristic while retiming and demultiplexing the data with no systematic phase offset. The receiver converts a 2.5 Gb/s $2^{23}-1$ PRBS NRZ signal into four 625 Mb/s signals. In addition to a low jitter, this receiver achieves a small chip area and power that is substantially lower than that of similar circuits. The high integration, low jitter and low power dissipation of this receiver IC and low cost of the CMOS process hold great promise for realizing this chip in optical communication system.

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