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Article

High-current MoS_2 transistors with non-planar gate configuration

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ABSTRACT

The ever-decreasing size of transistors requires effectively electrostatic control over ultra-thin semiconductor body. Rational design of the gate configuration can fully persevere the intrinsic property of two-dimensional (2D) semiconductors. Here we design and demonstrate a 2D MoS_2 transistor with omega-shaped gate, in which the local gate coupling is enhanced by the non-planar geometry. The omega-shaped non-planar transistors exhibit a high current of 0.89 A/μm and transconductance of 32.7 μS/μm. The high performance and desirable current saturation promise the construction of robust logic gate. The inverters show a voltage gain of 26.6 and an ideal total margin nearly 89%. We also assemble NOT-AND (NAND) gate on an individual MoS_2 flake, and the constructed NAND gate demonstrates the universal functionality of the transistors as well. This work provides an alternative strategy to fully take the advantages of 2D materials for high-performance field-effect transistors.

1. Introduction

Non-planar gate architecture promises an effective strategy for gate controllability enhancement because of excellent electrostatic control, which shows much better performance beyond conventional planar bulk technologies [1,2]. This structure offers the possibility for suppressing the short-channel effects with steep subthreshold swing (*SS*) as the continuously down scaling of transistors [3–5]. A wrap-around gate structure provides superior electrostatic gate control compared to planar structures [6,7]. As a consequence, the leakage current can then be suppressed while the device performance is still augmented. However, it requires complicated fabrication processes [8]. Namely, there is a compromise between the improvement in the electrostatic controllability and the fabrication complexity. An alternative solution to maximize the electrostatic confinement while minimizing the manufacturing complexity is to use an omega-shaped gate architecture, which possesses excellent electrical performance that induced by the improved gate controllability [2,9,10]. In the non-planar omega-shaped gate configuration, the semiconducting surface surrounded by the gate is increased in relation to the channel volume. The improvement of the electrostatic control offers low leakage and low power consumption for the field-effect transistors with ultra-short channel length (L_{ch}) [9]. However, 5 nm node silicon transistors require sub-3 nm body thickness for desirable channel control [11]. Traditional semiconductors are restricted by the mobility or quantum capacitance challenges at such ultra-thin body thickness. The imperfections of the traditional channel material surface scatter charge carriers, resulting in inferior current flow [12]. Moreover, the source-to-drain quantum tunneling or variability is pronounced and deteriorates the on–off ratio in scaled devices [13,14]. On the other hand, it is promising to apply other potential materials instead of silicon while scaling down the channel length of transistors [15–17]. Two-dimensional (2D) materials are crystalline sheets with atomic thickness. Due to the flat surfaces without dangling bonds, carriers are less prone to scattering and can flow relatively freely through the channel [18,19]. Therefore, 2D materials, such as MoS_2, represent the ultimately scaled transistors in large-area electronics [20]. Previously reported works mainly focus on shortening the planner dimension for ultra-short channel length, which demonstrates superior on-state channel current and verifies the competitive performance with that of the silicon-based transistors in some aspect. However, the reported planar MoS_2 field-effect transistors lack rational gate-coupling design, thus suffering from insufficient electrical performance [21–23].

In this work, non-planar MoS_2 field-effect transistors with omega-shaped gate configuration are fabricated. With the

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enhanced electrostatic coupling from the rational design of gate configuration, the transistors demonstrate robust performance with a high current of 0.89 mA/μm, high on–off ratio of 10^7 and a low threshold voltage (V_{TH}) of −2.85 V. Based on the excellent pinch-off and current saturation of the MoS_2 transistors, the NOT gate and NOT-AND (NAND) gate circuits are entirely assembled on an individual MoS_2 flake. The NOT gate inverters demonstrate a voltage gain of 26.6 at an applied voltage (V_{DD}) of 4.5 V and an almost ideal noise margin approaching $0.5V_{DD}$. And the constructed NAND gate indicates the universal functionality of the transistors. The strategy indicates a representative gate geometry design towards 2D electronics with competitive performance of silicon-based transistors.

2. Experimental

Few-layered MoS_2 can provide a balance between mobility and contact resistance of the device. Therefore, we adopt ~5 layers MoS_2 flakes as the channel layer in this work [24]. Fig. 1 schematically depicts fabrication process flow of our designed non-planar gate transistor. Firstly, the Ga_2O_3 nanowires (NWs) are prepared in a single zone horizontal tube furnace with chemical vapor deposition, which is similar with the previously reported works [25,26]. The Ga_2O_3 NW (the dimension D_{NW} ranges from 60 to 300 nm, Fig. S1 online) with Al_2O_3 dielectric layer was transferred onto 300 nm SiO_2 coated Si substrates, in which the Al_2O_3 dielectric layer is deposited via atomic layer deposition (ALD) approach [24]. And then the MoS_2 flake was transferred onto the nanowire by a physical dry transfer process [27]. Subsequently, ethyl alcohol was dipped onto the substrate and dried in air naturally to ensure the intimate contact between NW and MoS_2 flakes. The number of MoS_2 layers was confirmed by atomic force microscope image in Fig. S2 (online). Raman spectra based on the peak spacing between the E1 2g mode and the A_{1g} mode (Fig. S3 online), and the Raman spectra of the MoS_2 onto the Ga_2O_3 nanowire also present the consistent characteristic peak with that of the MoS_2 onto the SiO_2 substrate, indicating the strain is nearly released. The external source/drain region was defined by e-beam lithography, and Cr/Au electrode with a thickness of 10 nm/70 nm was deposited by thermal evaporator followed by the lift-off process, as shown in Fig. 1b [28]. ALD was employed to fabricate 15 nm top-gated Al_2O_3 dielectric, as shown in Fig. 1c. Fig. 1d is the schematic image of the fabricated omega-shaped gate MoS_2 transistor, in which the top gate Cr/Au electrode (10 nm/70 nm) was fabricated by beam lithography (EBL) followed by metal deposition and lift-off process. Fig. 1e is the cross-sectional schematic image of the gate architecture of the omega-shaped gate MoS_2 transistor. To reveal the effect of the gate configuration, finite element simulation was carried out by COMSOL Multiphysics. Fig. 1f is the corresponding finite element simulation of the electric field of the top gate. 2D model was created based on the structure of the fabricated device, and the electric field distribution was obtained by Semiconductor Module. The results indicate that the local electric field strength is enhanced by the non-planar gate configuration. The total top-gate capacitance (including simulated electrostatic capacitance and quantum capacitance) is calculated using electrostatic module and normalized by MoS_2 channel area, which is about 308.5 nF/cm^2.

3. Results and discussions

3.1. Electrical performance of the omega-shaped gate MoS_2 transistors

Fig. 2a is the scanning electron microscope (SEM) image of the top view of the omega-shaped gate MoS_2 transistors with channel length (L_{CH}) ranging from 150 nm to 2 μm. Fig. 2b shows typical transfer curves of the back-gated MoS_2 transistors with different buried D_{NW}, and D_{NW} is approximately equal to two times of the bending radius. As partial channel is separated by the nanowire from the back gate, the electrostatic coupling of the back gate is weakened for the devices with even larger D_{NW}. Therefore, the on–off ratio decreases with the increase of D_{NW}, which originates from the increased off-state current and decreased on-state current at larger D_{NW}. Fig. 2c is the evolution of the transfer characteristics of the omega-shaped gate MoS_2 transistors versus D_{NW}. All the devices present typical n-type characteristic with distinct pinch-off and an on–off ratio ~10^7. Typical hysteresis transfer characteristic of the transistors is shown in Fig. S4 (online). Due to the traps in dielectric layer, the gate capacitance does not follow gate voltage sweeping, leading to the hysteresis. Fig. 2d plots the variations of the transconductance (g_m) and V_{TH} versus D_{NW}. As the local gate field is enhanced by the omega-shaped gate configuration with the support of the nanowire, the g_m increases with D_{NW} below 180 nm. The maximum field-effect mobility is calculated to be 47.2 cm^2/(V s). Nevertheless, with the further increase of D_{NW},

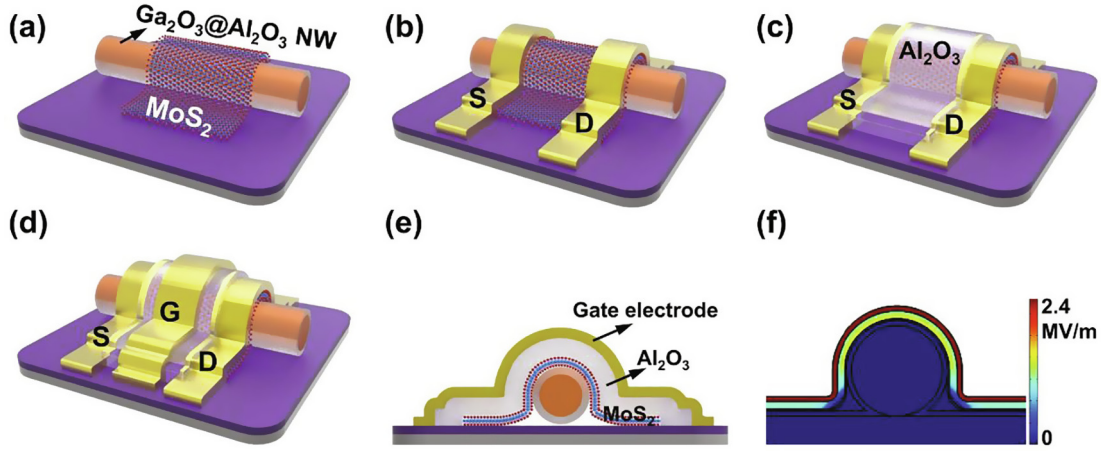

Fig. 1. Schematic illustrations of the fabrication processes of the MoS_2 transistors with omega-shaped gate. (a) Few-layer MoS_2 flake is transferred onto the Ga_2O_3 NW with Al_2O_3 dielectric layer, and etched with a fixed width of 1 μm. (b) The source/drain contact region is defined via e-beam lithography, Cr/Au (10 nm/70 nm) deposition with thermal evaporation and lift-off processes. (c) Al_2O_3 top-gated dielectric layer with a thickness of 15 nm is deposited by ALD. (d) The top-gate electrode region is defined by e-beam lithography, Cr/Au (10 nm/70 nm) deposition and lift-off processes. (e) Cross-sectional schematic image of the transistor. (f) The electric field distribution in the gate confirmation.

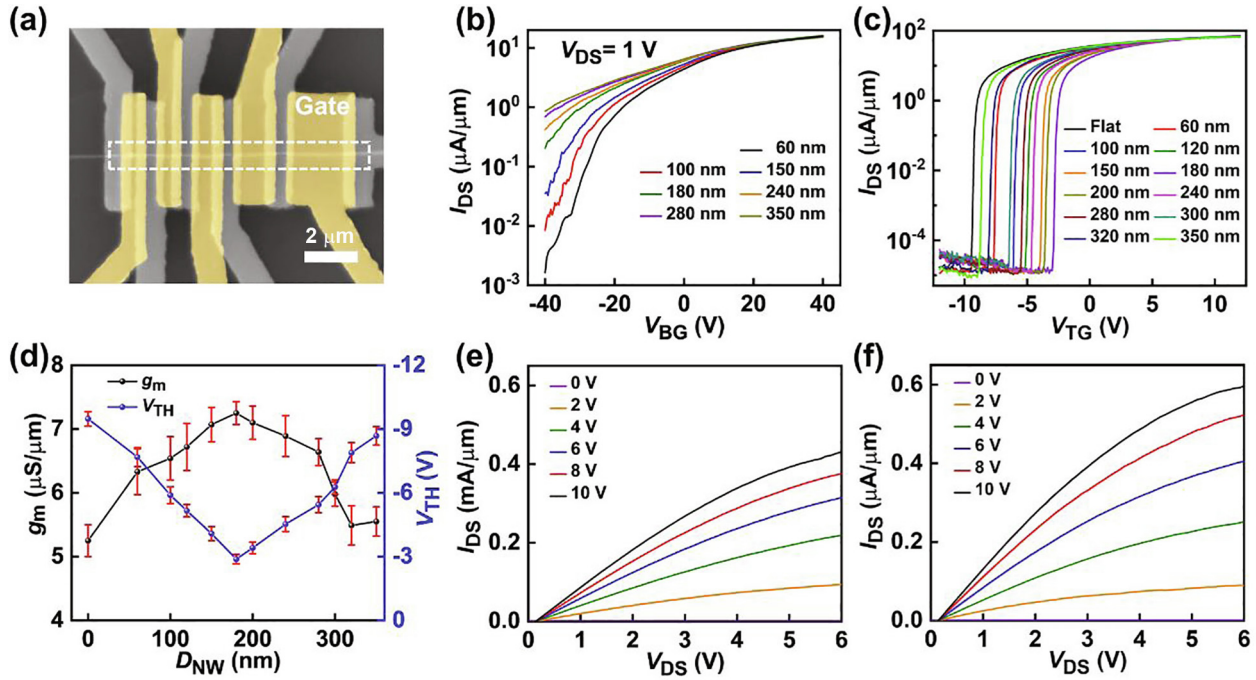

Fig. 2. Electrical performance of the omega-shaped gate MoS_2 transistors. (a) SEM image of the top view of the omega-shaped gate MoS_2 transistors. (b) Typical back-gated transfer characteristics of the omega-shaped gate MoS_2 transistors with different D_{NW}. (c) Typical top-gated transfer characteristics of the omega-shaped gate MoS_2 transistors with different D_{NW}, and the V_{DS} = 1 V for all the curves. (d) The plots of g_m and V_{TH} versus D_{NW}, and the statistical data are captured from the devices with a variation range of ±10 nm for D_{NW}. (e, f) The output characteristics of the MoS_2 transistors with planar (e) and omega-shaped (f) gate configuration, respectively.

the shape of the gate is approaching to planar, leading to degraded electrical performance that similar to the planar ones. Similarly, the V_{TH} of the devices is impacted by D_{NW}, which is induced by the D_{NW} dependent field distribution of the omega-shaped gate configuration [9,29]. Fig. 2e, f are the output curves of the MoS_2 transistors with planar and omega-shaped gate configuration (D_{NW} = 180 nm), respectively. The obvious pinch-off characteristics suggest that the MoS_2 active channel is fully modulated by the gate voltage. The largest output current of the planar and omega-shaped gate MoS_2 transistors are 0.47 and 0.59 mA/μm, respectively. Benefiting from ultra-thin body, the large bandgap of 1.2 eV and enhanced electrostatic control, channel current saturation and turn off is observed. These results indicate the present strategy is feasibility for enhancing the electrical performance of the MoS_2 transistors.

3.2. Electrical reliability of the short-channel omega-shaped top-gated MoS_2 transistors

We also investigate short-channel omega-shaped gate MoS_2 transistors. We adopt the MoS_2 flakes with similar thickness onto the nanowire with similar dimension to ensure a reliable comparison between the devices data. Fig. 3a presents typical transfer characteristics of fabricated devices. As the channel length shrinks, the on-state current is gradually increasing. Due to the short-channel effect (SCE), the devices obtain large V_{TH} values to pinch off the active channel. Transfer length method is used to extract contact resistance [30–32]. Fig. 3b is the plots of total channel resistance (R_T) as a function of channel length at V_{DS} = 1.0 V and V_{TG} = 12.0 V, which is the sum of two times of contact resistance (R_C) and channel resistance (R_{CH}). The R_C is about 0.9 kΩ μm under working condition, indicating that the contact resistance does not dominate the transport property of MoS_2 devices. Fig. 3c plots the g_m and SS versus L_{CH}. The g_m is increased as the channel length shrinks. In addition, the peak g_m of 32.7 μS/μm obtained at V_{DS} = 1.0 V is comparable with the previously reported values at a high V_{DS} = 5.0 V [21]. And due to the enhanced gate electrostatic coupling from the omega-shaped gate configuration, the devices with different channel lengths present steep subthreshold characteristic with a SS below 100 mV/dec as L_{CH} = 150 nm. Fig. 3d is the output current of the omega-shaped top-gated MoS_2 transistors with an L_{CH} = 150 nm. A maximum output current of 0.89 mA/μm is obtained, proving that the output current density has not been sacrificed for the diminution of L_{CH}. Table S1 (online) presents the performance comparisons among the MoS_2 transistors with similar channel length to state the significance of this work. And the current density of the MoS_2 is competitive with those in the previously reported work [33–35]. The sufficient current saturation in the omega-shaped top-gated MoS_2 transistors at short channel length is benefit for large voltage gain in circuits. Drain-induced barrier lowering (DIBL) is a short-channel effect in transistors referring originally to a reduction of threshold voltage of the transistor at higher drain voltages, which is induced by the electrostatic shield from the V_{DS} [36]. Fig. 3e is the transfer curves of the omega-shaped top-gated MoS_2 transistors with an L_{CH} = 150 nm. The residual leakage current in short channel devices as the V_{DS} is increased, and DIBL is 4.05 V for the devices with L_{CH} = 150 nm. Fig. 3f indicates the linear increment of I_{ON} as the L_{CH} decreasing. As the electrostatic screening from the V_{DS}, large V_{TG} is needed to pinch off the channel, leading to large V_{TH} values at high V_{DS}. These results indicate that the MoS_2 transistors with omega-shaped gate configuration show good immunity to short channel effects and potential for high-performance logic gate [36,37].

The direct-coupled field-effect transistor logic (DCFL) technology is a popular architecture for constructing low-power circuit [38]. As shown in Fig. 4a, in order to obtain high output current and transconductance, the gate region is fully over-lapping the channel, thus minimized parasitic and contact resistance can be persevered [23]. Fig. 4b is the corresponding circuit diagram of the fabricated devices. An inverter circuit is a basic logic element

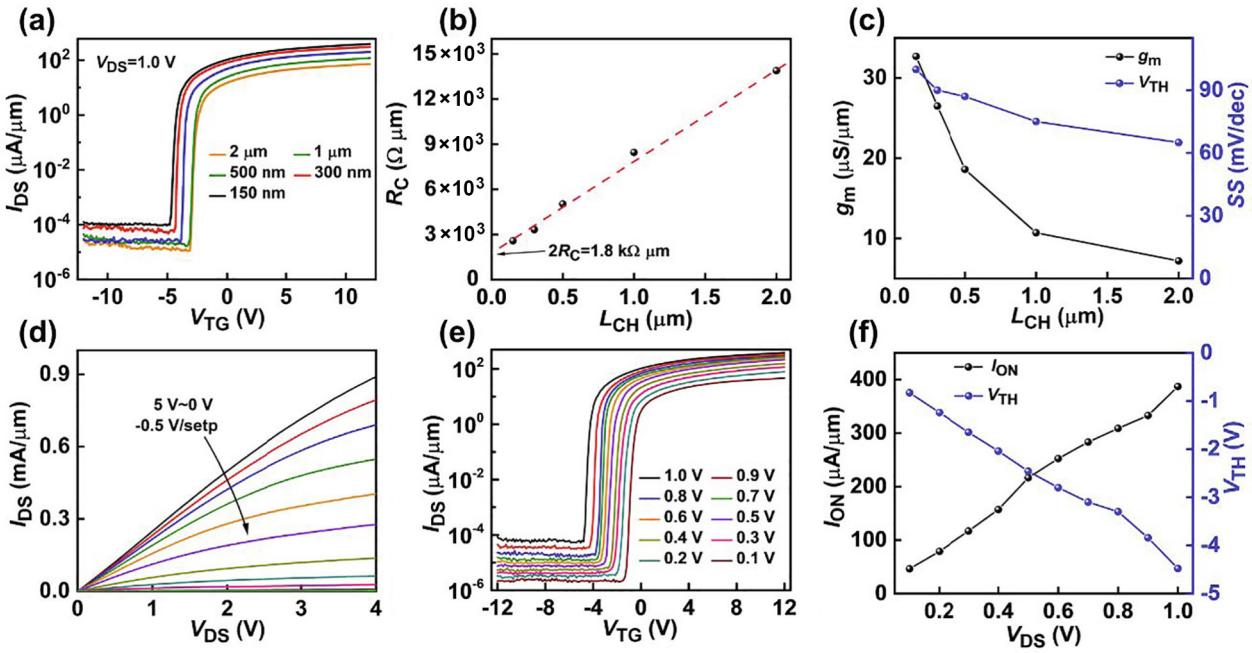

Fig. 3. Electrical reliability of the short-channel omega-shaped top-gated MoS_2 transistors. (a) Transfer curves of the omega-shaped top-gated MoS_2 transistors with different channel lengths. (b) Total channel resistance as a function of channel length at V_{DS} = 1.0 V and V_{TG} = 12.0 V. (c) The dependence of L_{ch} on g_m and *SS*. (d) Typical output current of the omega-shaped top-gated MoS_2 transistors with an L_{CH} = 150 nm. (e) Semi-log plot of the transfer characteristics with L_{CH} = 150 nm at different V_{DS}. (f) L_{CH} dependent I_{ON} and V_{TH} of the omega-shaped top-gated MoS_2 transistors.

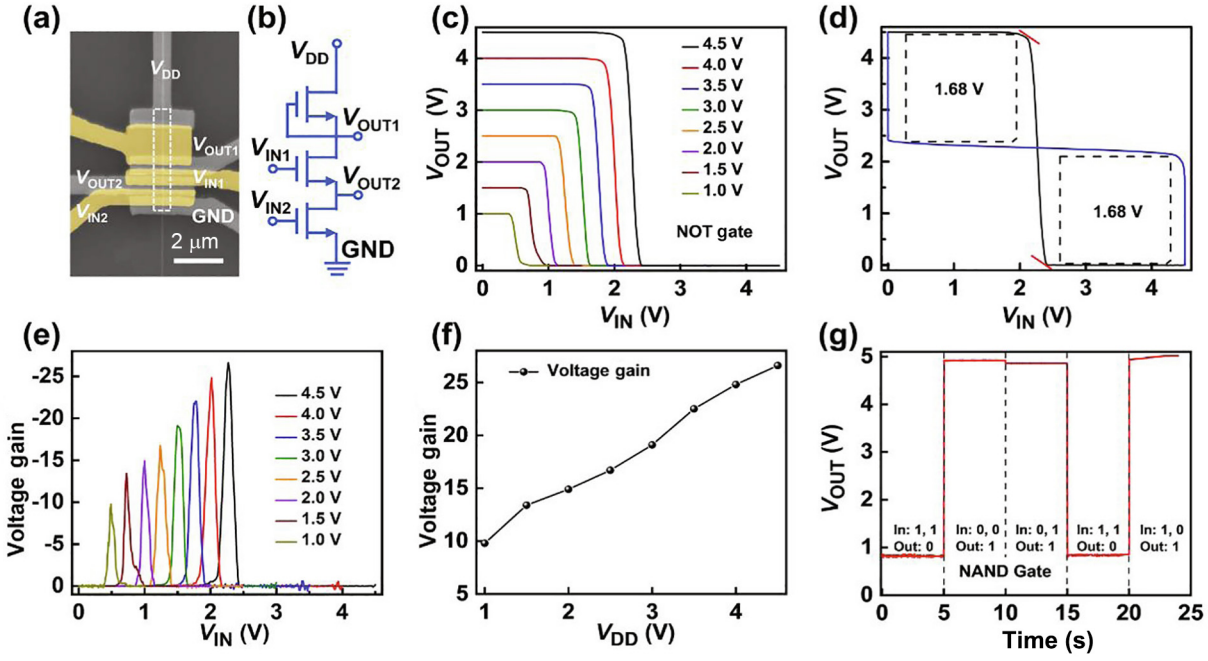

Fig. 4. Demonstration of integrated NOT and NAND logic gate. (a) SEM image of logic gate circuit. (b) Schematic of the electronic circuit for a logic inverter (when V_{OUT2} terminal is ground) and NAND (when V_{OUT2} terminal is suspending). (c) Output characteristics of the inverter at different V_{DD}. (d) Output voltage as a function of the input voltage and its mirror reflection. And noise margins ($NM_L = 0.45V_{DD}$, $NM_H = 0.44V_{DD}$) of the inverter. (e) Corresponding voltage gain of the inverter at different V_{DD}. (f) Voltage gain as a function of V_{DD}. (g) Output voltage of the NAND gate at different input states: (1, 1), (0, 0), (0, 1), (1, 1) and (1, 0). A low voltage of 0.1 V represents a logic state 0 and a voltage of 5 V represents a logic state 1.

that outputs a voltage representing the opposite logic-level to its input. When V_{OUT2} terminal is ground, it works as a logic inverter. And when V_{OUT2} terminal is suspending without any power connection, a NAND gate is constructed. Fig. 4c is the output characteristics of the inverter at different V_{DD}. The inverter exhibits sharp transition between high and low level. The noise margin is the maximum voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to deviate from the allowable logic voltage level. As shown in Fig. 4d, the high noise margins (NM_H) and

low–noise margins (NM_L) are extracted from the voltage transfer characteristic and its mirror reflection curve, and $NM_L = 0.45V_{DD}$ and $NM_H = 0.44V_{DD}$ are obtained, indicating the robustness of the inverter towards noise. The inverter demonstrates a total margin nearly 89% and an almost ideal noise margin of 0.5 at V_{DD} = 4.5 V. Fig. 4e is the voltage gain of the inverter that calculated by taking the derivation of the voltage transfer curves. Fig. 4f indicates the voltage gain increases with increasing V_{DD} and a voltage gain 26.6 is achieved at V_{DD} = 4.5 V. In Fig. 4g, the output voltage of the NAND gate is measured as a function of time while the two input voltage states vary across all four possible logic combinations (1,1), (0,0), (0,1) and (1,0). The results demonstrate robust NAND gate functions that constructed with the omega-shaped top-gated MoS_2 transistors.

4. Conclusion

In summary, we mainly focus on enhancing the local gate field coupling of the MoS_2 transistors by introducing an omega-shaped top-gated configuration. Owing to the improved gate controllability from the sharpened corner geometry, the top-gated devices exhibit good immunity to short channel effects, current saturation at short channel length, reliable operation. NOT and NAND gate with robust functions are constructed based on the desirable transistor performance, and the inverter indicates nearly ideal noise margins and high voltage gain. The strategy presents a rational design of the gate geometry and is an alternative avenue to promote high-performance low-power applications for 2D materials.

Conflict of interest

The authors declare that they have no conflict of interest.

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Author contributions

Xingqiang Liu and Lei Liao conceived and designed the experiments. Jun Lin prepared the manuscript. Bin Wang and Guoli Li finished numerical simulation related parts, and also contributed to analysis and interpretation of results. Zhenyu Yang fabricated the MoS_2 back-gated devices, and the related characterizations and measurements. Yang Chai and Xuming Zou presented the suggestions for improving the quality of this work and revised the manuscript. Top-gated devices related tests and result analysis were done by Jun Lin using protocols provided by Lei Liao. All authors examined and commented on the manuscript.

Appendix A. Supplementary materials

Supplementary materials to this article can be found online at https://doi.org/10.1016/j.scib.2020.12.009.

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