Science Bulletin 68 (2023) 3102–3104

Contents lists available at ScienceDirect

Science Bulletin

journal homepage: www.elsevier.com/locate/scib

Research Highlight

Advanced hybrid 2D/CMOS microchips toward the semiconductor industry

Fei Hui [a,*], He Tian [b,*]

[a] School of Materials Science and Engineering, Zhengzhou University, Zhengzhou 450001, China
[b] School of Integrated Circuits and Beijing National Research Center for Information Science and Technology (BNRist), Tsinghua University, Beijing 100084, China

Most of today's integrated circuits, known as chips or microchips, are fabricated using complementary metal–oxide–semiconductor (CMOS) technology. Conventional CMOS devices (mainly referred to as Si-based transistors) have reached their fundamental physical limits and are facing energy-efficient challenges. Therefore, it is difficult to scale them down further, primarily due to the challenges concerning short-channel effect, quantum effects, etc. In contrast, atomically thin two-dimensional (2D) materials, such as graphene, transition metal dichalcogenides (TMDs), and hexagonal boron nitride (h-BN), exhibit unique mechanical, electrical, thermal, and optical properties, allowing the further scaling down in the device dimensions and the reduction of power consumption [1,2]. Moreover, hybrid integration is more attractive as it can benefit from multiple materials and combine their advantages together [3]. For example, several attempts have been made to integrate graphene into radio-frequency device with multiple-functions, while the integration density is still low and cannot meet the requirements of semiconductor industry [4]. Ref. [5] reported a hybrid hardware integrating 2D MoS_2 synapses with CMOS neurons to achieve character recognition with high accuracy (98.8%) and low evergy consumption (11.4 μW). Therefore, the introduction/integration of 2D materials in electronic devices would highly enable its potential application for high-density chips with enhanced performance.

Up to now, various mechanical-exfoliated 2D materials-based prototype devices (e.g., transistors, memristors, sensors) have been constructed in the labs and most of them presented enhanced performances with promising applications in the fields of optoelectronics, bio-medicine, among others [6–8]. For the semiconductor industry, 2D materials, were proposed as a potential solution by IEEE International Roadmap for Devices and Systems (IRDS) (the 2021 edition). Furthermore, some world-leading institutes/companies in the field of the semiconductor industry, such as IMEC [9], TSMC [10], Intel [11], have implemented the exploitation of 2D materials in CMOS technology, to explore its possibilities in current sub 10 nm-node CMOS chips and for neuromorphic computing. However, the scalable fabrication of 2D materials remains a big challenge aiming for its implementation in the semiconductor industry. On the other hand, most of reported works have shown prototype devices of 2D materials, few of them present the abilities of data storage and compute in a real microchip. Moreover, low yield and low reliability/variability are also main issues existing in most of the reported devices to hinder the steps of 2D materials-based electronics moving from Lab-to-Fab [12]. The hybrid 2D/CMOS microchips remain elusive [13].

In a recent paper [14], the authors successfully constructed hybrid 2D/CMOS microchips by transferring chemical vapor deposition (CVD) synthesized h-BN (18-layer-thick, ~6 nm) onto the back-end-of-line interconnections of silicon microchips that contain CMOS transistors of the 180 nm node, enabling its large-scale integration, high parallelism and more complex operations for future data-intensive chips. In this work, a 2 cm × 2 cm microchip, containing (without a passivation layer) 5 × 5 crossbar arrays of one-transistor-one-memristor (1T1M) cells (Fig. 1a), was separated from a 200 mm silicon wafer fabricated in a standard CMOS foundry. Compared with common fabrication methods (e.g., mechanical exfoliation, solution-processed approach), this work employed scalable CVD (a more reliable method and scaled up to chip integration) to obtain wafer-scale thin h-BN layer, and transferred it onto target 1T1M crossbar arrays, following by top Au-Ti electrodes deposition (Fig. 1b). And the correct layered structure of h-BN and construction of Au-Ti-h-BN-W memristor (as small as ~0.053 μm^2) on the exposed conductive tungsten (W) via have been further demonstrated by high-angle annular dark-field cross-sectional transmission electron microscope (TEM, Fig. 1c). Herein, good electrical contacts between 2D h-BN and the W vias have been confirmed by etching the native oxides of the as-received crossbar array. Given the successful demonstrations of wafer-scale hybrid h-BN/CMOS microchips, it is noted that vdW materials can even be directly embedded in silicon chip by a precise transfer process or can be post-fabricated on a silicon chip through layer-by-layer stacking [15].

Electrical measurements conducted on both standalone Au-Ti-h-BN-W and hybrid Au-Ti-h-BN-W/CMOS devices present erratic current–voltage (I–V) characteristics (no resistive switching) and typical non-volatile resistive switching behaviors, respectively, revealing that the transistors in CMOS provide a precise and effective control over the current across the h-BN-based memristors.

* Corresponding authors.
E-mail addresses: feihui@zzu.edu.cn (F. Hui), tianhe88@tsinghua.edu.cn (H. Tian).

https://doi.org/10.1016/j.scib.2023.11.034

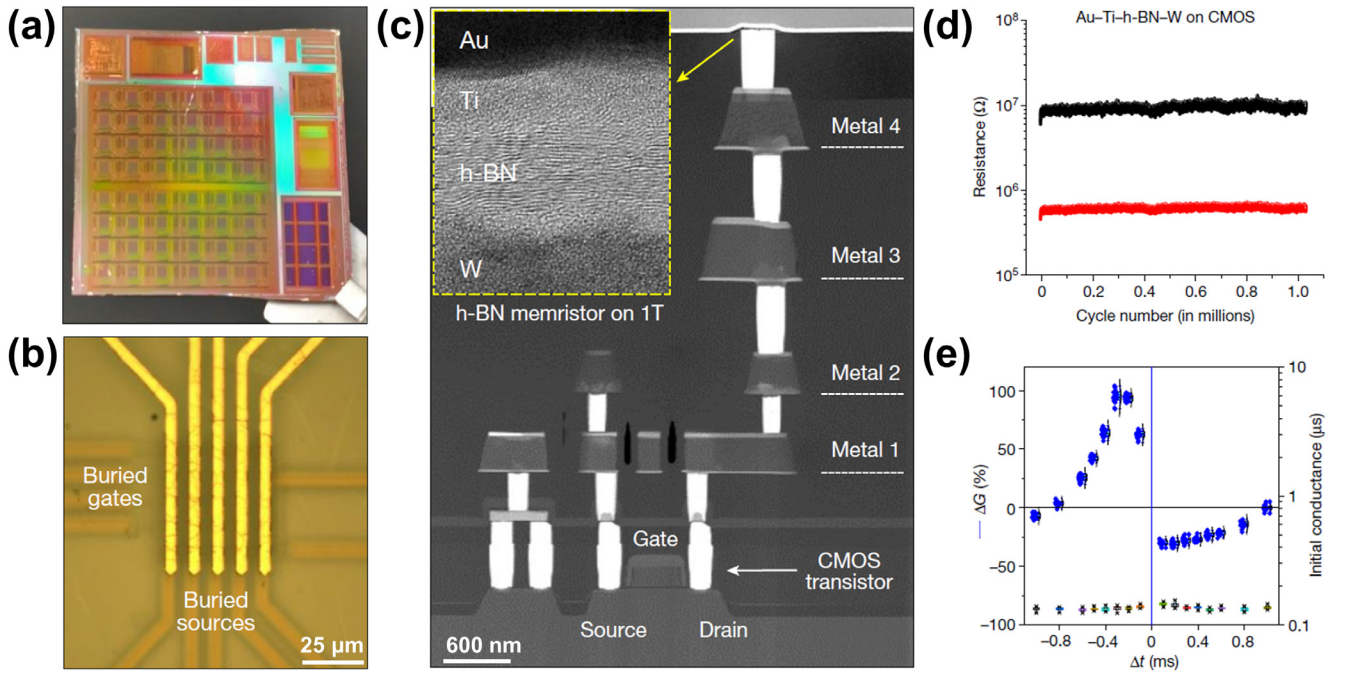

Fig. 1. (Color online) (a) Photograph of 2 cm × 2 cm microchips containing the CMOS circuitry. (b) Optical image of a 5 × 5 crossbar array of 1T1M after transferring a 6 nm-thick h-BN layer and depositing top Au electrodes. (c) High-angle annular dark-field cross-sectional transmission electron microscope (TEM) image of a 1T1M cell in the crossbar array. The inset (20 nm × 16 nm) shows a cross-sectional TEM image of the Au–Ti–h-BN–W memristor on the via. (d) Endurance plot of 1T1M cell showing around 1 million cycles for write pulse duration of 1 ms. (e) STDP characteristics of the 1T1M cell with Au–Ti–h-BN–W memristor, before STDP characterization, the devices are always tuned to the same initial conductance (lower box charts, which relate to the right *y* axis). Figures are reproduced from Ref. [14], Copyright © 2023, Springer Nature.

Moreover, by applying sequences of pulsed voltages stresses (PVS) and tuning write pulse durations from 0.1 to 1 ms, the fabricated hybrid h-BN/CMOS devices could show high endurance up to ~5 million cycles with adjustable R_{HRS}/R_{LRS} ratio (Fig. 1d). The obtained ultra-high endurance in such small memristors (~0.053 μm^2) is quite competitive with the commercial metal-oxide-based resistive random-access memories (0.5 million cycles, Fujitsu). The authors also estimated the properties of the 1T1M cells using different top electrodes (i.e., Au, Ag), revealing a reliable switching at lower state resistances, shorter switching time and lower switching energy when Au electrodes are used solely, and the values of the above parameters can be further reduced when Ag electrodes used, especially the switching energy down to 1.41 pJ, due to higher conductivity and diffusivity of Ag ions. This provides researchers with strategies for choosing appropriate electrodes and designing novel device structures.

Note that this work also proves the hybrid h-BN/CMOS 1T1M cells show good potential for data computation by applying pairs of PVS. The results demonstrate in-memory computation using the 5 × 5 crossbar array and present spike-timing dependent plasticity (STDP) signals (Fig. 1e) that are suitable for the implementation of spiking neural networks (SNN). Furthermore, by fitting the measured STDP and device-to-device variability data, h-BN-based memristors successfully implement unsupervised learning rules with a very high accuracy up to 90%. Moreover, it needs to highlight that the programming voltages in the h-BN-based memristors are around ±1.4 V, which are much lower than most commercial Flash memories (20 V), bipolar-CMOS microchips for automotive applications (40 V), as well as prototype memristive devices developed by companies (±5 V).

Pure CMOS technology still suffers from the scaling limit and energy consumption. Developing 2D technology can enable further scaling down with low energy consumption. There are two strategies to develop the 2D/CMOS electronics. One is Front end of line (FEOL), but 2D materials may not survive the rest potential high temperature processes. The other is back end of line (BEOL). This article proofs the BEOL is an effective way to enable the integration of 2D electronics with CMOS. Future challenge can be large-scale integration of 2D electronics with CMOS. Overall, this work is not only extremely helpful to promote the development of high-integration-density 2D/CMOS hybrid microchips, especially in the aspects of scaling limit and energy consumption, but also represents a significant advance for 2D neuromorphic devices with high reliability and low variability toward the semiconductor industry. Instead of prototype electronic circuits presented in most literature, this work successfully achieved in-memory computation in 2D materials-based industrial microchips with high endurance, initially realizing the Lab-to-Fab of 2D semiconductor devices, and presenting promising to extend the Moore's Law. This is a groundbreaking that accelerates the application for semiconductor companies and breaks the wall of energy-hungry electronics. However, we are still at the early stage of the development for the integration of 2D materials in semiconductor industry, and numerous fundamental challenges (e.g., scalable growth methods compatible with CMOS technology, high-uniformity, high device yield and high reliability) still need to be addressed before these materials can meet the standards for industrial applications.

Conflict of interest

The authors declare that they have no conflict of interest.

References

[1] Lemme MC, Akinwande D, Huyghebaert C, et al. 2D materials for future heterogeneous electronics. Nat Commun 2022;13:1392.
[2] Wen C, Li X, Zanotti T, et al. Advanced data encryption using 2D materials. Adv Mater 2021;33:2100185.

[3] Resta G, Leonhardt A, Balaji Y, et al. Device and circuits using novel 2-dimensional materials: a perspective for future VLSI systems. IEEE Trans Very Large Scale Integr (VLSI) Syst 2019;27:1486–503.
[4] Han S, Garcia AV, Oida S, et al. Graphene radio frequency receiver integrated circuit. Nat Commun 2014;5:3086.
[5] Xue S, Wang S, Wu T, et al. Hybrid neuromorphic hardware with sparing 2D synapse and CMOS neuron for character recognition. Sci Bull 2023;68:2336–43.
[6] Kanungo S, Ahmad G, Sahatiya P, et al. 2D materials-based nanoscale tunneling field effect transistors: current developments and future prospects. npj 2D Mater Appl 2022;6:9590.
[7] Wang M, Cai S, Pan C, et al. Robust memristors based on layered two-dimensional materials. Nat Electron 2018;1:130–6.
[8] Bolotsky A, Bueler D, Dong C, et al. Two-dimensional materials in biosensing and healthcare: from *in vitro* diagnostics to optogenetics and beyond. ACS Nano 2019;12:9781–810.
[9] Schram T, Sutar S, Radu I, et al. Challenges of wafer-scale integration of 2D semiconductors for high-performance transistor circuits. Adv Mater 2022;34:2109796.
[10] Lee TE, Su YC, Lin BJ, et al. Nearly ideal subthreshold swing in monolayer MoS_2 top-gate nFETs with scaled EOT of 1 nm. IEEE IEDM 2022, San Francisco, USA, https://ieeexplore.ieee.org/document/10019552.
[11] O'Brien KP, Naylor CH, Dorow CJ, et al. Process integration and future outlook of 2D transistors. Nat Commun 2023;14:6400.
[12] Lanza M, Smets Q, Huyghebaert C, et al. Yield, variability, reliability, and stability of two-dimensional materials based solid-state electronic devices. Nat Commun 2020;11:5689.
[13] Goossens S, Navickaite G, Monasterio C, et al. Broadband image sensor array based on graphene-CMOS integration. Nat Photonics 2017;11:366–71.
[14] Zhu K, Pazos S, Aguirre F, et al. Hybrid 2D-CMOS microchips for memristive applications. Nature 2023;618:57–62.
[15] Li M, Liu H, Zhao R, et al. Imperfection-enabled memristive switching in van der Waals materials. Nat Electron 2023;6:491–505.

Fei Hui is an Associate Professor of Zhengzhou University in China. She got her Ph.D. degree in Nanoscience at University of Barcelona and Chemistry at Soochow University in 2018. During 2016−2017, she also studied at the Massachusetts Institute of Technology and the University of Cambridge as a visiting student. In 2018−2021, she was a postdoctoral fellow at Technion – Israel Institute of Technology. Her research interest is two-dimensional materials and nanoelectonics.

He Tian received his Ph.D. degree from the Institute of Microelectronics, Tsinghua University in 2015. He is currently an Associate Professor and Deputy Director at Institute of Integrated Electronics, School of Integrated Circuits, Tsinghua University. His current research interest includes various 2D material-based devices.