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A compact SCR model using advanced BJT models and standard SPICE elements

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Dear editor,

The Silicon controlled rectifiers (SCR) are widely used to protect integrated circuits (ICs) from electrostatic discharge (ESD) and electrical overstress (EOS) damage [1]. An accurate SCR model is highly desirable in on-chip ESD protection design. Previous studies modeled SCRs by aggregating conventional bipolar junction transistor (BJT) models and adding extra physical models that conventional BJT models fail to support [2,3]. However the auxiliary models are mostly complicated and need much efforts to develop in behavioral languages like Verilog-A.

Meanwhile, developing new models based only on existing SPICE models is efficient and highly flexible [4,5]. Using advanced MOSFET and BJT models, these aforementioned works have successfully modeled MOS and modified SCRs respectively. However, in conventional SCR's equivalent circuit, only BJTs exists and their inherent weak-avalanche models are insufficient to model collector-base junction breakdown [6]. Moreover, because of conventional SCR's unique conduction mechanism, the impedance change caused by collector currents should also be modeled [2]. To solve these problems, this paper added some standard SPICE elements into the equivalent circuit and developed a compact conventional SCR model that supports both transmission line pulse (TLP) and direct current (DC) measurements.

Model description. A general description of the conventional SCR is shown in Figure 1(a) in solid lines. The equivalent SCR circuit consists of one PNP transistor, one NPN transistor and two resistors, R_P and R_N. In order to extend model with high current effects, such as Early effect and high injection effect, Mextram models for BJTs are used in this work. However, more physical phenomena should be included to form a compact SCR model.

Junction breakdown is critical in modeling SCR's unique snapbacks performance. Regarding conventional SCR modeling, no auxiliary MOSFET structure is embodied in its equivalent circuit and the weak-avalanche models in Mextram BJTs [6] are shown as

$$I_{\text{weak-avl}} = I_c \frac{A_n}{B_n} \lambda_D E_M \left\{ \exp\left(-\frac{B_n}{E_M}\right) - \exp\left[-\frac{B_n}{E_M}\left(1+\frac{W_{\text{eff}}}{\lambda_D}\right)\right]\right\}, \tag{1}$$

$$E_M = \frac{1}{2}\left(E_W + E_0 + \sqrt{(E_W - E_0)^2 + 0.1E_{\text{av}}^2 \frac{I_{\text{cap}}}{I_{\text{HC}}}}\right), \tag{2}$$

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where I_c is the collector current without avalanche, E_M is the maximum electric field, λ_D is the intersection point, W_{eff} is the effective epilayer width, E_W is the electric field at the end of the epilayer, E_0 is the absolute electric field, I_{cap} is a function of the critical current at velocity saturation, I_{HC} and the collector current I_C, and E_{av} is the average electric field at the base-collector junction.

Since I_c is quite low before snapback triggering, the corresponding weak-avalanche currents are not sufficient to model snapback triggering [6]. Hence, the additional avalanche breakdown model should be considered. In 2012, Hajjar et al. [7] proposed a non-physical description of bipolar breakdown which is formed by a combination of resistances, diode and constant voltage source to extend the capability of BJT models.

This paper proposes a junction avalanche breakdown model by integrating one standard diode, one constant voltage source and one voltage controlled resistance (VCR) together (shown in the dashed box in Figure 1(a)). And the calculation of collector current before triggering can be given as

$$I_{\text{triger-avl}} = I_S\left[\exp\left(\frac{q(V_{\text{dio}} - V_{\text{Th-dio}})}{nkT}\right) - 1\right], \quad (3)$$

$$V_{\text{dio}} = V_{\text{CB}} - V_T - I_{\text{triger-avl}}R_{\text{dio}}, \quad (4)$$

where I_S is the saturation current, V_{dio} is the voltage over standard diode, $V_{\text{Th-dio}}$ is the threshold voltage of standard diode, V_{CB} is the voltage over collector-base junction, R_{dio} is the series resistance of diode and its expression will be introduced in (5). Eqs. (3)–(5) together form the junction breakdown model of SCR, and work as the main source to describe snapback triggering.

When voltage over SCR reaches breakdown voltage, currents traveling through R_P and R_N will increase radically, resulting in voltage drops on well resistances and forward bias of BJTs. Then the SCR is triggered. The junction breakdown voltage is determined by summing up the value of constant voltage source (V_T) and the threshold voltage of standard diode (D_T), while R_{dio} represents junction resistance before and after avalanche breakdown. The reason why R_{dio} performs as a VCR is due to the impedance change of SCR, which will be explained in detail later. All these three parameters can be extracted from reverse biased junction current-voltage (I-V) curve.

Another factor greatly influences SCR snapbacks is the impedance variation during ESD events [3]. As shown in Figure 1(b), a part of PNP transistor's collector current accompanied with plenty of minority carriers flows to p-type substrate, and consequently leads to an increase of majority carrier concentration. With the aid of condensed majority carriers, base resistance and current gain of parasitic NPN transistor are largely reduced and enhanced respectively, transferring SCR into low impedance state. By introducing a p-i-n diode model, Ref. [3] successfully developed compact models to support both high-impedance and low impedance working states. However, these models are quite complicated and need extensive efforts to develop in Verilog-A.

As shown in Figure 1(a), this paper proposes an impedance transformation model by adding two VCRs, i.e., R_D and R_{dio}, into the SCR's equivalent circuit. Their mathematic expressions are linear piecewise functions described in (5) and (6),

$$R_D = \begin{cases} R_{\text{high-impedence}} - R_{Pn} - R_{\text{junction}}, & V_{Rn} < V_{\text{Th-pnp}}, \\ (R_{\text{high-impedence}} - R_{Pn} - R_{\text{junction}})\,\frac{V_{\text{on-pnp}} - V_{Rn}}{V_{\text{on-pnp}} - V_{\text{Th-pnp}}}, & V_{\text{Th-pnp}} < V_{Rn} < V_{\text{on-pnp}}, \\ 0, & V_{Rn} > V_{\text{on-pnp}}, \end{cases} \quad (5)$$

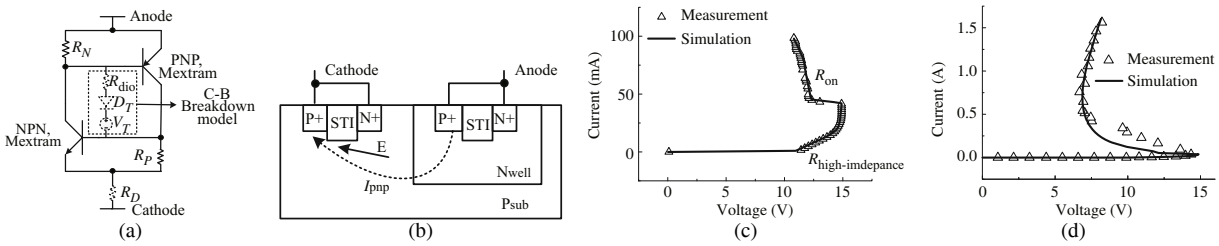
$$R_{\text{dio}} = \begin{cases} R_{\text{junction}}, & V_{Rn} < V_{\text{Th-pnp}}, \\ R_{\text{on}} + (R_{\text{junction}} - R_{\text{on}})\,\frac{V_{\text{on-pnp}} - V_{Rn}}{V_{\text{on-pnp}} - V_{\text{Th-pnp}}}, & V_{\text{Th-pnp}} < V_{Rn} < V_{\text{on-pnp}}, \\ R_{\text{on}}, & V_{Rn} > V_{\text{on-pnp}}, \end{cases} \quad (6)$$

where V_{Rn} is the voltage drop over R_n, R_{junction} is diode resistance before triggering, R_{on} is diode resistance after triggering, $R_{\text{high-impedance}}$ is the SCR impedance before triggering, R_{pn} is the total resistance of R_n and R_p, $V_{\text{Th-pnp}}$ is the threshold voltage of PNP, $V_{\text{on-pnp}}$ is the PNP base-emitter voltage when SCR is fully triggered.

When V_{Rn} is below PNP transistor threshold voltage, the values of R_D and R_{dio} stay high, indicating the SCR is in high impedance state. As V_{Rn} goes higher, the PNP transistor is turned on and R_D together with R_{dio} gradually decreases. When V_{Rn} is high enough, the SCR changes to low impedance state eventually. Therefore, the impedance variation of SCR is modeled.

As for parameter extraction, $R_{\text{high-impedance}}$ and R_{on} are extracted by analyzing DC I-V curve of the SCR (shown in Figure 1(c)), as well as $V_{\text{Th-pnp}}$ and $V_{\text{on-pnp}}$. The well resistances, R_n and R_p, are extracted from the snapback trigger voltage in the snapback curves measured with TLP (shown in Figure 1(d)).

In brief, the compact conventional SCR model mainly consists of Mextram BJT models, a junc-



Parameter	Value (V)	Parameter	Value (Ω)	Parameter	Value (Ω)
$V_{Th\text{-}dio}$	0.7	R_{pn}	36	R_{on}	70
V_{CB}	10.9	$R_{junction}$	125	$R_{high\text{-}impedance}$	211

(e)

Figure 1 Model description and verification. (a) General SCR equivalent circuit (solid lines) and new compact model (solid and dashed lines); (b) mechanism of SCR impedance change; (c) measured and simulated DC I-V characteristics of SCR; (d) measured and simulated TLP I-V characteristics of SCR; (e) values of extracted model parameters.

tion breakdown model (described by (3)–(5)) and an impedance variation model (formed by (5) and (6)).

Model validation. A conventional SCR with a width of 40 μm was fabricated in a standard 65-nm CMOS process for model extraction and measurement. The parameter extraction results are listed in Figure 1(e). By implementing in SPICE simulator, the proposed SCR model has been verified against measurements. Figure 1(d) shows measured and simulated TLP I-V characteristics. Excellent match can be seen before snapback triggering and in high current region. Some mismatches occur in the points right after triggering. In these points, the triggering current was quite low and the SCR needed more time to switch to a fully-on state. Therefore, the current and voltage curves in the sampling region, i.e., 70–90 ns, were not steady [8]. While the sampled currents were increasing, the sampled voltages decreased slowly from triggering voltage to holding voltage.Consequently, the voltage of these points appeared to be higher than the simulation results.

Although most SCRs are mainly focused on protecting chips from ESD damage, EOS events are also of great importance in IC design. Since most EOS pulses are accompanied with slow rising edges which resemble DC charging, a validation of DC test is depicted in Figure 1(c). Good correlation is found between measurement and simulation. Meanwhile, the variation of SCR impedance under different current injection conditions is clearly shown and verified with measurement. Indicating the compact model is capable of performing slow rising edge pulse characterization, and supporting DC-based design and EOS design.

Conclusion. We have presented a compact SCR model for ESD protection. The work illustrated an efficient and flexible approach to develop a conventional SCR model by integrating various standard SPICE models together. Meanwhile, detailed model description and extraction of key parameters are presented. In addition to TLP test validation, the presented model demonstrates the effectiveness in DC characterization which is of benefits in EOS design.

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