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Citation: SCIENCE CHINA Information Sciences **54**, 767 (2011); doi: 10.1007/s11432-011-4205-z

View online: https://engine.scichina.com/doi/10.1007/s11432-011-4205-z

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Published by the Science China Press

SCIENCE CHINA
Information Sciences

• RESEARCH PAPERS •

April 2011 Vol. 54 No. 4: 767–777
doi: 10.1007/s11432-011-4205-z

Scan chain design for shift power reduction in scan-based testing

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Received August 11, 2009; accepted December 1, 2009; published online February 28, 2011

Abstract Test power of VLSI systems has become a challenging issue nowadays. The scan shift power dominates the average test power and restricts clock frequency of the shift phase, leading to excessive thermal accumulation and long test time. This paper proposes a scan chain design technique to solve the above problems. Based on weighted transition metric (WTM), the proposed extended WTM (EWTM) that is utilized to guide the scan chain design algorithm can estimate the scan shift power in both the shift-in and shift-out phases. Moreover, the wire length overhead of the proposed scan chain design can also be reduced by the proposed distance of EWTM (DEWTM) metric. Experimental results confirm that the proposed approach can significantly reduce scan shift power with low wire length overhead.

Keywords low power DfT, scan-based testing, test power reduction, scan chain design

Citation Li J, Hu Y, Li X W. Scan chain design for shift power reduction in scan-based testing. Sci China Inf Sci, 2011, 54: 767–777, doi: 10.1007/s11432-011-4205-z

1 Introduction

Conventional very large scale integration (VLSI) systems are usually implemented to provide both high performance and integration, which brings many new challenges. Among these challenges, power dissipation is a very important one [1]. Test power may be twice as high as the power consumed during the normal function mode [2], because: 1) Unlike successive functional input vectors applied to a given VLSI system, which usually have significant correlations, the correlations between consecutive test patterns are usually loose. 2) Test engineers usually use parallel testing in the VLSI system to reduce the test application time and thus cut down the test cost, which results in excessive power dissipation in the long duration of shift phase.

Scan-based test techniques dominate the current design-for-testability (DfT) market, but they suffer from increasing power dissipation caused by excessive transitions during the long shift process, which will create unnecessary transitions in the cores under test. This high test power may make the system fail or damaged during the test phase, or affect its long term reliability [3]. Moreover, it will also limit the test frequency and hamper the test parallelism of multiple cores in the system. Therefore, the demand of low power during testing increases rapidly.

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Many DfT modification techniques have been proposed for scan shift power reduction recently, which can be broadly categorized into two types:

(1) Vector-independent techniques: Scan partitioning [4, 5] can suppress the scan chain rippling. Gates insertion between the scan chain and the combinational portion of the circuit [6] can reduce scan shift power at the cost of the degradation of functional performance due to additional gate delay. Scan chain clustering [7–9] can reduce the scan shift power with some design overhead. The above techniques do no need to be particularly designed according to their test vectors.

(2) Vector-dependent techniques: Scan chain redesign [10–15] can significantly reduce the number of switching activities on scan chains thus cutting down the scan shift power. And logic gate insertion between scan cells was proposed in [16]. Though these techniques need to be particularly used for each design according to their different test vectors, their efficiencies are usually much higher than that of vector-independent technique with much less performance degradation.

There are also other low power techniques without DfT modification [17–19]; however, they are usually not so efficient on shift power reduction as the above techniques.

This paper proposes a DfT modification technique for reducing the shift power through scan chain design. Based on previous weighted transition metric (WTM) [20], extended WTM (EWTM) is proposed to estimate the scan shift power caused by transitions in each scan cell. Distance of EWTM (DEWTM) is also proposed to shorten the scan wire connection. In the proposed algorithm, we first divide the scan cells into two scan chains according to signal-0 and signal-1 probabilities of their stimuli and responses, and then in each partitioned scan chain, order the scan cells by the proposed EWTM and DEWTM.

The rest of this paper is organized as follows: Preliminaries will be given in the next section. Section 3 illustrates the proposed EWTM. Section 4 introduces the proposed scan design, and DEWTM is introduced in section 5 to shorten the scan wire connection. Section 6 discusses some practical issues of vector-dependent DfT techniques including the proposed one. Finally, section 7 reports experimental results, and section 8 concludes this paper.

2 Preliminaries

Power dissipation in CMOS circuits consists of two parts: dynamic and static. Dynamic power dissipation occurs during output switching because of short-circuit current, and charging and discharging of load capacitance, while static power dissipation is caused by leakage current or other currents continuously drawn from the power supply. For existing CMOS technology, dynamic power is the dominant source of power dissipation, though it may change soon with developing technology.

Dynamic power dissipation of CMOS circuit can be calculated as

$$P_{\text{dynamic}} = \frac{1}{2} C_{\text{load}} V_{DD}^2 f \alpha, \tag{1}$$

where f is the clock frequency, α is the expected number of output transitions in a clock period, C_{load} is the load capacitance (including gate input and interconnect capacitances), and V_{DD} is the supply voltage of the circuit. By eq. (1), under given C_{load}, V_{DD} and f, which are usually decided by given technology and design, the most efficient and easy way to reduce dynamic power is to reduce the value of α, which has linear correlation with the dynamic power dissipation.

There are two major phases in scan-based testing schemes: shift and capture. Capture cycles appear periodically among shift cycles, and shift cycles are usually hundreds of times of capture cycles. The main target of this paper is to reduce power dissipation during shift mode, because: 1) Low correlations among successive patterns during the shift phase make the switching activities much higher and irregular than that of normal mode. Though instantaneous power dissipation during capture cycles are usually higher than that of shift cycles, the duration of shift mode is usually much longer than that of capture mode, the accumulated thermal effect may induce serious structural degradations, such as hot spots, corrosion, electro-migration, hot-carrier-induced defects, or dielectric breakdown. 2) On the other hand, to avoid these damages, engineers usually have to slow down the shift clock thus further raising the test cost; in

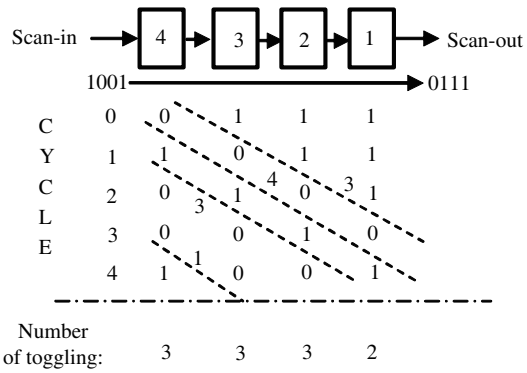


Figure 1 Transitions on scan chain caused by test stimuli and responses.

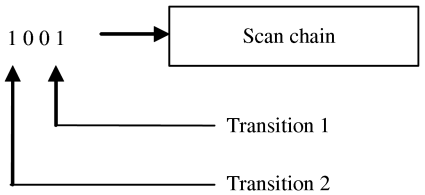


Figure 2 Transitions in test stimuli.

other words, we can cut down the test cost by reducing shift power so as to enhance the required shift cycle frequency. 3) Existing capture power reduction techniques usually resort to X-filling techniques without conflicting with the proposed DfT technique, as has been proven in prior works [17–19] and will also be verified in experimental results of this paper.

Ref. [20] showed that power dissipation of the system under test has nearly linear correlation with the transition count happening in the scan cells. Transitions caused by the shift operation are decided by the logic value differences between adjacent bits in the test vector as shown in Figure 1. In this scan chain, the test response vector shifted out of the scan chain is '0111', and the next test stimulus vector shifted into the scan chain is '1001'. Transitions caused by logic value differences in the test vectors in each cycle are all highlighted by dot lines.

3 Extended weighted transition metric

To estimate dynamic power in the shift-in or shift-out phases shown in Figure 1 efficiently and quickly, ref. [20] proposed weight transitions metric (WTM). Consider a scan chain of length l and a scan vector $V_i = V_{i,1}V_{i,2}V_{i,3}V_{i,l}$ with $V_{i,1}$ scanned in the scan chain before $V_{i,2}$, and so on, the WTM of the vector is

$$WTM_i = \sum_{j=1}^{l-1}(V_{i,j} \bigoplus V_{i,j+1}) \times (l-j). \tag{2}$$

For the example scan chain in Figure 2, the test stimulus vector that will be shifted into the scan chain is 1001, there are two logic value differences within this vector, and the transition count caused by these two logic value differences are different during the shift phase: Transition 1 will cause three scan cells to toggle and transition 2 will cause only one scan cell to toggle as can be verified in Figure 1.

It has also been shown in [20] that the power dissipation of the system under test has nearly linear correlation with transitions that happen in the scan chain. Therefore, if the entire test cube contains N_v stimulus vectors, the average scan-in power $P - in_{\text{avg}}$ can be estimated as

$$P - in_{\text{avg}} = \frac{\sum_{i=1}^{N_v}[\sum_{j=1}^{l-1}(V_{i,j} \bigoplus V_{i,j+1}) \times (l-j)]}{N_v}. \tag{3}$$

Power dissipation during the shift phase also consists of two parts: scan-in and scan-out. Similar formulae can also be used for scan-out power estimation.

However, the above calculation can only estimate the consumed shift power in either shift-in or shift-out phase, but not both. Therefore, we need to extend it so as to estimate transitions caused by logic value differences in both test stimuli and responses when the shift-in and shift-out are conducted in parallel as shown in Figure 1. Different from WTM, which is used to calculate transitions caused by a test vector, EWTM can calculate transitions that happen between two scan cells according to their logic values in

both test stimulus and response vectors in the whole test set, which can help to decide proper connection order of these scan cells.

In Figure 1, there is one logic value difference within the response vector $R_i = R_{i,1}R_{i,2}R_{i,3}R_{i,4}$= '1110', and two logic value differences in the next test stimuli vector V_{i+1}= '1001'. The logic value difference in the response vector will cause transitions at three scan cells: $Cell_1 - Cell_3$, while the two logic differences in the stimulus vector make 3 scan cells ($Cell_2 - Cell_4$) and one scan cell ($Cell_4$) toggle respectively. Notice that the logic value differences between $R_{i,3}$ and $R_{i,4}$ and $V_{i+1,3}$ and $V_{i+1,4}$ are both caused by different logic values between $Cell_3$ and $Cell_4$, but these logic differences have different impacts on scan chain transitions during the shift phase. The former one causes three cells to toggle during scan-out, while the latter one only causes $Cell_4$ to toggle during scan-in. Additionally, notice that there is another kind of transitions induced by different logic values between the last bit of response vector and the first bit of stimulus vector, which causes power dissipation at all the scan cells. This kind of transitions can be reduced by scan vector reordering, which is not emphasized in this work but is also interesting. If the test cube contains N_v pairs of stimulus and response vectors, $EWTM_j$ between a pair of adjacent scan cells $Cell_j$ and $Cell_{j+1}$ can be calculated as

$$EWTM_j = WTM_j^{\text{shift-in}} + WTM_j^{\text{shift-out}} = \sum_{i=1}^{N_v}(V_{i,j} \bigoplus V_{i,j+1}) \times (l-j) + \sum_{i=1}^{N_v}(R_{i,j} \bigoplus R_{i,j+1}) \times j, \quad (4)$$

where j ranging from 1 to $l-1$ stands for position of the scan cell nearer to the scan-out port in this pair of scan cells.

Based on (3) and (4), the average shift power (including both shift-in and shift-out power) dissipation can be estimated as

$$P_{\text{shift}} = \frac{\sum_{j=1}^{l-1}[\sum_{i=1}^{N_v}(V_{i,j} \bigoplus V_{i,j+1}) \times (l-j) + \sum_{i=1}^{N_v}(R_{i,j} \bigoplus R_{i,j+1}) \times j] + \sum_{i=1}^{N_v-1}(R_{i,l} \bigoplus V_{i+1,1)\times l}}{N_v}. \quad (5)$$

By (3)–(5), the power dissipated during scan test depends not only on logic value differences among stimuli or responses, but also on the sum of their respective weights.

The major difference between WTM and EWTM is: WTM measures the transitions occurring in the scan chain in a horizontal way, which calculates the transitions happening within a test vector; while EWTM considers the transitions in a vertical way, which focuses on the total transitions during the entire test phase caused by test stimuli and responses of the test cube between two adjacent scan cells, so their placement can be adjusted according to EWTM.

4 Proposed scan chain design

From the previous analysis, we can see that shift power reduction can be achieved by reducing EWTM between scan cell pairs in scan chains. To this end, the proposed low power scan chain design goes in two steps: first, grouping the scan cells according to the signal-0 and signal-1 probabilities of their test stimuli and responses; second, ordering the scan cells according to their EWTM.

4.1 Scan cell grouping

Generally speaking, a scan cell may contain different numbers of '0' and '1' bits in its test stimuli and responses. If one scan cell contains more '1's in its test stimuli and responses, but its adjacent scan cells contains more '0's, or vice versa, there will probably be more transitions in the scan chain. Therefore firstly, to reduce logic value differences between adjacent scan cells in scan chains, we assign these scan cells to two groups according to their stimulus and response signal probabilities.

Considering the test set shown in Figure 3, where $S_1 - S_5$ denote 5 test stimulus vectors and $R_1 - R_5$ denote the 5 test response vectors, signal probabilities of 0 and 1 of each scan cell can be calculated according to their logic values in these test vectors as

# Scan cell	1	2	3	4	5	6	7	8	9	10
S_1	*X*	*X*	*X*	*X*	*X*	1	1	1	0	*X*
R_1	1	*X*	0	*X*	*X*	*X*	*X*	0	0	1
S_2	0	0	1	0	1	*X*	0	*X*	*X*	*X*
R_2	1	1	0	1	0	0	1	*X*	0	1
S_3	*X*	0	1	1	1	1	0	1	1	0
R_3	0	1	0	1	1	1	1	1	0	1
S_4	*X*	0	1	0	0	1	1	1	0	*X*
R_4	1	0	1	0	0	*X*	*X*	*X*	*X*	*X*
S_5	*X*	*X*	1	1	0	1	1	*X*	1	0
R_5	1	0	1	0	0	0	0	*X*	*X*	*X*
P_1	0.4	0.2	0.6	0.4	0.3	0.5	0.5	0.4	0.2	0.3
P_0	0.2	0.5	0.3	0.4	0.5	0.2	0.3	0.1	0.5	0.2
Group ID	1	0	1	0	0	1	1	1	0	1

Figure 3 Signal probabilities of 0 and 1 of scan cells.

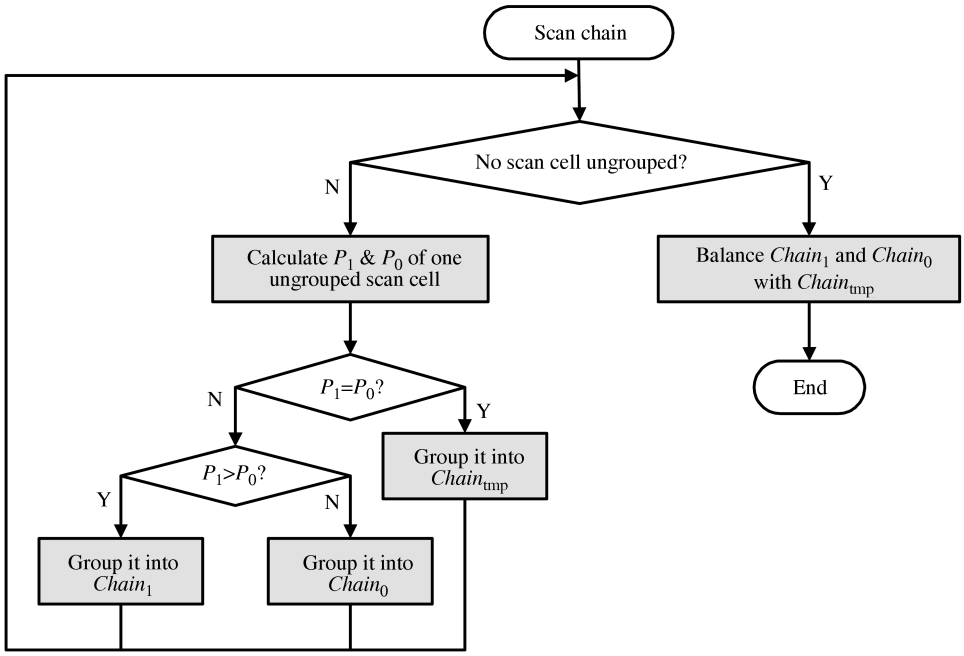
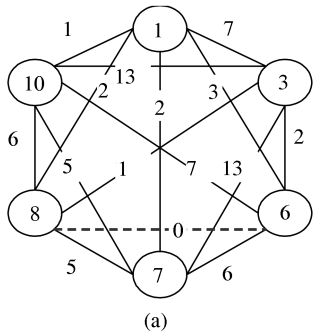


Figure 4 Scan cell grouping decision flow chart.

$$P_{1/0} = \frac{\sum_{i=1}^{n}(i = 1/0)}{n}, \tag{6}$$

where n is the number of test vectors. The results are shown behind P_1 and P_0 in Figure 3. Now we can assign scan cells in the system to two groups according to P_1 and P_0 so that scan cells in the same group are more likely to have the same logic value: scan cells with higher P_1 are assigned to one group called $Group_1$, and scan cells with higher P_0 are grouped into $Group_0$.

As shown in Figure 3, $\{Cell_1, Cell_3, Cell_6, Cell_7, Cell_8, Cell_{10}\}$ are grouped into $Chain_1$, and $\{Cell_2$, $Cell_5$, $Cell_9\}$ are grouped into $Chain_0$. After grouping the scan cells that have different P_1 and P_0, the scan cells with equal P_1 and P_0 will be assigned to the scan chain with fewer scan cells to balance length of these two scan chains to achieve a shorter test time. For example, the 4th scan cell in Figure 3 will be assigned to the scan chain with fewer scan cells, and it is $Chain_0$ in this case. The flow of our scan cell grouping is outlined in Figure 4.



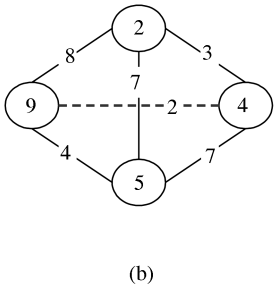


Figure 5 Cost graphs. (a) Cost graph of $Group_1$; (b) cost graph of $Group_0$.

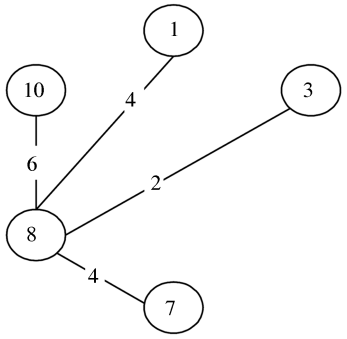


Figure 6 Cost graph of $Group_1$ for finding $Cell_3$.

In practice, scan chains are usually firstly segmented according to modules. In that case, our scan cell grouping can be conducted within each module to reduce test power of itself and the entire system.

4.2 Scan cell ordering

Besides reducing the count of logic value differences in scan chains, we also try to reduce the shift transition counts caused by these logic value differences, which is mainly decided by the connection order of scan cells in each scan chain. Therefore, after the scan cell grouping process demonstrated in the previous section, we will decide connection orders of scan cells in $Group_1$ and $Group_0$ according to the proposed EWTM to form two scan chains: $Chain_1$ and $Chain_0$.

By (4), for a given position, where j is a constant, $EWTM_j$ is only relative to $\sum_{i=1}^{N_v}(V_{i,j} \oplus V_{i,j+1})$ and $\sum_{i=1}^{N_v}(R_{i,j} \oplus R_{i,j+1})$, but their weights are not equivalent. $\sum_{i=1}^{N_v}(V_{i,j} \oplus V_{i,j+1})$ has a weight of $(l-j)$, while $\sum_{i=1}^{N_v}(R_{i,j} \oplus R_{i,j+1})$ has a weight of j.

To decide the connection order of the scan cells in $Group_1$ and $Group_0$ constructed in the scan cell grouping procedure, we have to calculate the EWTM value for each pair of the scan cells in the same group, and put the scan cells into the positions to achieve the minimum scan shift transition count.

For example, Figure 5(a) shows the cost graph for scan cells in $Group_1$ from Figure 3. Each vertex represents a scan cell SC_i, and because all the grouped scan cells are not ordered yet, we need to calculate $EWTM_1$ between each pair of the scan cells, shown as the weight of each edge in the cost graph. Because $EWTM_1$ between SC_6 and SC_8 is 0, they are first ordered into $Chain_1$ as $Cell_1$ and $Cell_2$. Here we choose SC_6 as $Cell_1$ and SC_8 as $Cell_2$, and then delete $Cell_1$ (SC_6) in this figure. The first two scan cells in $Chain_0$ can also be decided similarly as shown in Figure 5(b), which will be SC_4 and SC_9 in this example.

Next we need to decide $Cell_3$ in $Chain_1$. Since $Cell_1$ (SC_6) has been deleted, $EWTM_2$ between $Cell_2$ (SC_8) and the scan cell not ordered are recalculated as shown in Figure 6. We can find that if SC_3 is put adjacent to SC_8, there will be fewer transitions, and the decision process for $Cell_3$ in $Chain_0$ is similar. This iteration will continue until all the scan cells grouped into these scan chains have all been ordered.

After deciding connecting order of the scan cells, X-bits in test stimuli can be easily filled with low-power X-filling techniques [17–19] to further reduce possible scan shift or capture transitions.

5 Wire length consideration

Scan cell ordering in subsection 4.2 does not consider the distance between adjacent scan cells, which may cause long scan wire length. Therefore, we take scan wire length into account in this section. We first use EDA tools (here we use Cadence Encounter) to obtain placement information of each scan cell. Then the Manhattan distance $D_{i,j}$ between each pair of scan cells is

$$D_{i,j} = |X_i - X_j| + |Y_i - Y_j|, \tag{7}$$

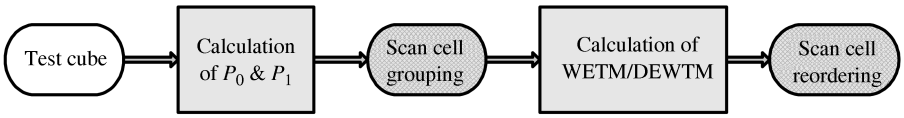


Figure 7 Proposed low power DfT design flow.

where X_i, X_j and Y_i and Y_j are x- and y-coordinates of these two scan cells, respectively.

Now, distance of EWTM (DEWTM) is proposed to estimate the co-effect of distance and EWTM among the scan cells. DEWTM_j between the jth and the $(j+1)$th scan cell can be calculated as

$$DEWTM_j = \frac{\alpha_D D_{i,j}}{D_{\max}} + \frac{\alpha_T EWTM_j}{EWTM_{\max}}, \tag{8}$$

where i ranges all the scan cells that have not been ordered into the scan chain yet; α_D and α_W are co-efficiencies of distance and EWTM between two scan cells, respectively, ranging from 0 to 1, and the sum being 1. They can be utilized by DfT engineers to make a tradeoff between reduction of transitions in the scan chain and the wire length of the scan chain. $D_{\max}$ and $EWTM_{\max}$ are used to unify the effect of distance and EWTM between two scan cells, so that the terms after α_D and α_W can be both between 0 and 1.

$D_{\max}$ means the maximum distance between any two scan cells in the circuit, calculated as

$$D_{\max} = \max\{|X_{\max X} - X_{\min X}| + |Y_{\max Y} - Y_{\min Y}|, |X_{\max Y} - X_{\min Y}| + |Y_{\max Y} - Y_{\min Y}|\}, \tag{9}$$

where $X_{\max X}$ and $Y_{\max X}$ are the x- and y-coordinate of the scan cell with the maximum x-coordinate, $X_{\min X}$ and $Y_{\min Y}$ are for the scan cell with the minimum x-coordinate; and similar to $X_{\max Y}$, $Y_{\max Y}$, $X_{\min Y}$ and $Y_{\min Y}$.

The maximum EWTM between any two scan cells is

$$EWTM_{\max} = j \times N_v + (l - j) \times N_v = l \times N_v, \tag{10}$$

where l and N_v are the number of scan cells of the system and vectors in the test set, respectively.

Now, during the scan cell ordering phase, the weights in the cost graph are DEWTMs now to guarantee fewer scan shift transitions with shorter scan wire connection.

The flow of our low power DfT design can be concluded now as shown in Figure 7. In the first phase, P_0 and P_1 of each scan cell are calculated by eq. (6), and scan cells are grouped into two scan chains: $Chain_0$ and $Chain_1$ according to the comparison between their P_0 and P_1. In the second phase, in each scan chain, the scan cells are reordered according to the calculation of EWTM or DEWTM. Then the scan architecture is formed.

6 Practical discussions

Though vector-dependent DfT techniques (including the proposed one) can reduce shift power significantly with a low overhead, they also suffer from several practical problems.

1. Work with test compression: Test compression is widely applied in current DfT flow, and our technique can work well with it. Because the proposed technique is only concerned about test bits finally transferred into the scan cells, as long as we can obtain the test set after the decoder logic of the test compression scheme, both lower test data volume and shift power can be achieved.

2. Drawback: Such vector-dependent techniques still face one problem: the DfT structure needs redesigning whenever there are changes in the hardware and the test set. However, when the change is small, the shift power still could be reduced, though some efficiency may be sacrificed without redesigning the scan chain.

Table 1 Statistical information for experimental circuits

Circuit	#Scan cells	#Test vectors	X%
s5378	179	111	71.35%
s9234	211	159	72.79%
s13207	638	236	93.23%
s15850	534	126	83.66%
s38417	1636	99	67.80%
s38584	1426	136	82.48%

Table 2 Test power reduction and wire length overhead of the proposed technology without consideration of the wire length

Circuits	Average shift		Average capture		Wire length	
	Ori.	Prop.(Red.%)	Ori.	Prop.(Red.%)	Ori.	Prop.(Incre.%)
s5378	731415	244379(66.6%)	93	54(41.9%)	10101	10393(2.9%)
s9234	2020705	510123(74.8%)	78	62(20.5%)	14945	14284(−4.4%)
s13207	14301591	3923762(72.6%	210	152(27.6%)	223852	235485(5.2%)
s15850	8608253	2358846(72.6%)	181	149(17.7%)	145888	150303(3.0%)
s38417	87115769	42492976(51.2%)	383	246(35.8%)	2445002	2424988(−0.8%)
s38584	102615050	3224207(96.9%)	680	572(15.9%)	1709203	1719043(0.6%)
Average	35898797	8792382(72.4%)	271	206(26.6%)	758165	759083(1.1%)

7 Experimental results

To verify the efficiency of our method, we conduct experiments on full-scan version of several ISCAS'89 benchmark circuits, and these designs are synthesized with 0.18 μm technology libraries by Synopsys Design Compile, and the scan chains are routed by Cadence Encounter. MinTest [21] test sets are used for these circuits (The don't-care bits are not filled in the ATPG procedure).

Two sets of experiments have been conducted on full-scan version of larger ISCAS'89 benchmark circuits using our low power DfT scheme under different configurations. One is performed without considering the wire length overhead; the other takes the wire length into consideration with the proposed DEWTM metric. These two sets of experiments are described in details in the following subsections. Table 1 presents general information about the benchmarks and test cubes used to evaluate our scheme: the number of scan cells, test vectors and X bit percent are all provided under "# Scan cells", "# Test vectors" and "X%", respectively.

7.1 Experiments without consideration of wire length

In the first set of experiments, we have constructed the proposed scan architecture without considering the wire length overhead to obtain the maximum test power reduction ratio. Two steps as illustrated in section 4 under guidance of EWTM are applied during the constructing, and for X-bits left in the test cube after the proposed scan chain design, they are filled arbitrarily with X-filling technique for capture power reduction (the method in [18] is adopt in this experiment; however, there is no dependency between the X-filling procedure and the proposed technique, so any other X-filling techniques can also be applied for different capture power reduction efficiencies).

Table 2 lists the average test power (including both the shift power and the capture power) reduction results and the wire length overheads of such scan chain designs. The average shift power and capture power of the original and the proposed scan chain design are measured by EWTM under "Ori." and "Prop." below "Average shift" and "Average capture", respectively. And the test power reduction of the proposed technique against the original scan chain design of these circuits are given in brackets ("Red.%") under "Prop.". The wire length increments of the proposed scan chain design of these circuits are listed under "Prop.(Incre.%)" to show the overhead of the proposed technique.

Table 3 Peak test power reduction of the proposed technology without consideration of the wire length

Circuits	Peak shift		Peak capture	
	Ori.	Prop.(Red.%)	Ori.	Prop.(Red.%)
s5378	121	86(28.9%)	154	103(33.1%)
s9234	129	72(44.2%)	103	108(−4.9%)
s13207	554	315(43.1%)	264	267(−1.1%)
s15850	468	286(38.9%)	241	246(−2.1%)
s38417	1468	841(42.7%)	587	545(7.2%)
s38584	871	597(31.5%)	767	747(2.6%)
Average	602	377(38.2%)	353	336(5.8%)

From Table 2 we can see that, compared with the average test power reduction ratio (72.4% for shift power and 26.6% for capture power, in which the capture power reduction is mainly due to the efficiency of X-filling technique), the wire length overhead of the proposed technique is very low (1.1% on average), and this wire length overhead can be further reduced with the guidance of DEWTM, as will be verified in the next subsection.

For completeness, the peak power (including both peak shift power and peak capture power) results are also listed in Table 3. As can be seen from this table, the peak shift power can also be significantly reduced by the proposed scan chain design. However, because the proposed scan chain are constructed without considering the capture power, some patterns in some circuits may have higher peak capture power than the original design, but due to efficient X-filling after the scan chain design, the average peak capture power can be reduced in the experimental circuits.

7.2 Experiments with consideration of wire length

To reduce the wire length overhead of the proposed technique, the second set of experiments is conducted as illustrated in section 4. The only difference between this set of experiments and the previous one is that the guidance is DEWTM now; thus the wire length can be considered and reduced during the scan chain construction.

In order to show the effectiveness of the weights in DEWTM: α_T and α_D, we have conducted two sets of configurations of these two values: (1) α_T=0.1 and α_D=0.9, which means the transition count between two scan cells is more important than the location consideration of them in the reordering process; (2) α_T=0.9 and α_D=0.1, which means that the distance between two scan cells are more important in the reordering.

Figure 8 shows the effectiveness of DEWTM on reducing the wire length of the scan chains of the experimental results. In this figure, the first set of data "1" shows shift/capture power reduction and wire length increment of the proposed technique with guidance of EWTM (results shown in the previous subsection); the second set of data "2" shows the above values of configuration (1) as illustrated in the previous paragraph; and the third set of data "3" shows the above values of configuration (2) as illustrated in the previous paragraph.

As is evident in this figure, with only little loss of test power reduction ratio, the wire length overhead drops steeply as shown in the trend of the green line.

8 Conclusions

This paper has addressed the test power problem in scan-based environments in systems where this problem is acute due to the scan chain transitions during the shift of test data, and proposed a low power DfT scheme to solve it. This approach has been shown to be both effective and easy to implement with low wire length overhead. There are two phases in the proposed method: scan cell grouping and reordering: 1) grouping: The scan cells are grouped into two scan chains according to the possibilities of 0 and 1 of logic value of this scan cell in a given test cube; 2) reordering: The scan cells in respective scan chain are reordered according to two metrics proposed in this paper to achieve fewer transition that

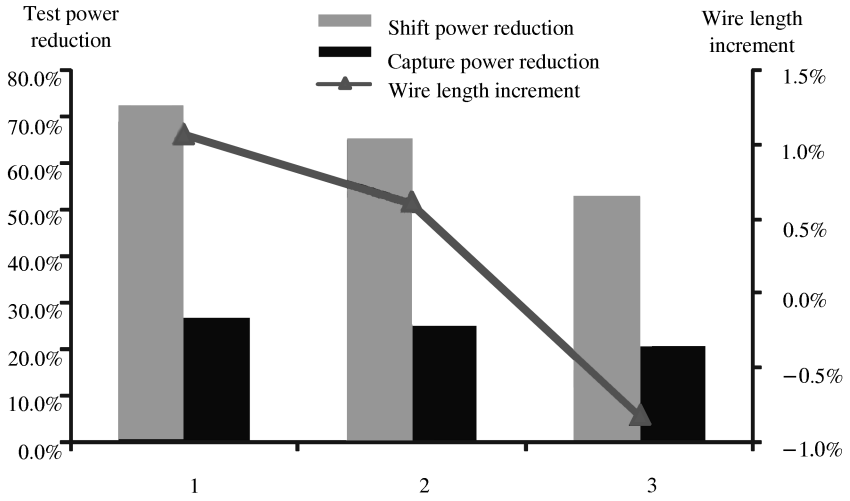


Figure 8 Wire Length Reduction with DEWTM.

happen in the scan chain with low wire length overhead. Two metrics are proposed to guide the scan cell reordering process: extended weighted transition metric (EWTM) used to estimate transitions caused by different logic values between both test stimulus and response bits in two adjacent scan cells, and distance of extended weighted transition metric (DEWTM) used to estimate the co-effect of distance and EWTM between scan cells.

Experimental results show that the proposed scan chain design can achieve high shift power reduction with low wire length overhead, which can still be further reduced by scan chain construction with guidance of the proposed DEWTM. Moreover, there is still space for X-filling to accomplish for capture power reduction after the proposed scan chain design, as has been verified in the experiments.

The future work will focus on the routing congestion problem of our design. In addition, test power during the capture cycles is also an important concern of test power problem in scan-based scheme, which will be co-optimized with shift power in our future work. Moreover, as leakage power has become more and more important in recent years, it is also to be considered.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant Nos. 60633060, 60803031, 61006017), the National Basic Research Program of China (Grant No. 2005CB321604), the National High-Tech Research & Development Program of China (Grant Nos. 2007AA01Z107, 2007AA01Z113, 2007AA01Z109, 2009AA01Z129), the National Science Foundation of China (Grants Nos. 60425203, 60910003), the Key Laboratory of Computer System and Architecture, ICT, CAS (Grant No. ICT-ARCH200902), and China Postdoctoral Science Foundation (Grant No. 20100470014).

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