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4-channel, 40 Gb/s front-end amplifier for parallel optical receiver in 0.18 μm CMOS

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Abstract This paper proposed a 4-channel parallel 40 Gb/s front-end amplifier (FEA) in optical receiver for parallel optical transmission system. A novel enhancement type regulated cascade (ETRGC) configuration with an active inductor is originated in this paper for the transimpedance amplifier to significantly increase the bandwidth. The technique of three-order interleaving active feedback expands the bandwidth of the gain stage of transimpedance amplifier and limiting amplifier. Experimental results show that the output swing is 210 mV (Vpp) when the input voltage varies from 5 mV to 500 mV. The power consumption of the 4-channel parallel 40 Gb/s front-end amplifier (FEA) is 370 mW with 1.8 V power supply and the chip area is 650 μm × 1300 μm.

Keywords enhancement type regulated cascade (ETRGC), active inductor, transimpedance amplifier, limiting amplifier, three-order interleaving active feedback

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1 Introduction

With characteristics such as large capacity and high speed data rate, optical fiber communication has developed rapidly in network and multimedia applications. Parallel transmission is an important method to increase the speed of optic-fiber communication integrated circuits, at the same time it has the advantage of simple structure and short latency time over serial interconnects. In synchronous communication system, optical signal has become very week in the receiving end after traveling dozens or even hundreds of kilometers. The front-end amplifier (FEA) aims to convert the week current pulse from PD to a certain limiting voltage signal and introduce noise as little as possible.

A low power FEA is designed in TSMC 0.18 μm CMOS technology in this paper, which consists of transimpedance amplifier (TIA) and limiting amplifier (LA). The FEA is the most critical element in an optical receiver affecting the whole system performance such as speed, sensitivity, and signal-to-noise ratio. Hence, the design mandates careful optimization of a number of tradeoffs among bandwidth, gain, and noise. For high speed application, some broadband techniques are employed in circuit design. In TIA, the input stage adopts a novel enhancement type regulated cascade (ETRGC) configuration with an active inductor to expand bandwidth, while the gain stage chooses three-order interleaving active feedback to acquire a high gain and broad bandwidth at the same time. In LA, three-order interleaving active feedback is also employed in the core units.

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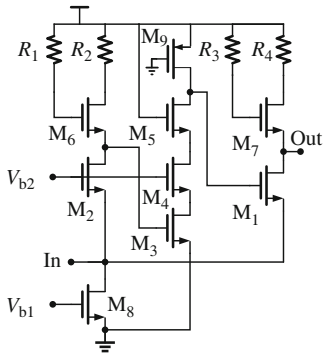


Figure 1 Circuit of input stage.

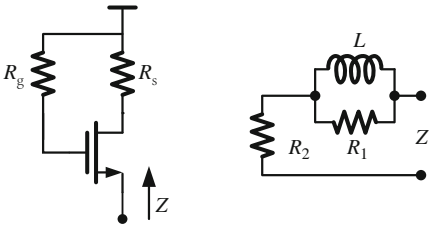


Figure 2 Circuit and equivalent model of active inductor.

2 TIA design

The front-end amplifier (FEA) consists of transimpedance amplifier (TIA) and limiting amplifier (LA). TIA is aimed to convert a week current from PD to voltage signal, and the voltage signal will be further amplified by the following LA. The TIA is constructed by the input stage and the gain stage.

2.1 Input stage

As the first stage of TIA as well as the front-end amplifier, the input stage has to convert current signal to voltage. To reduce the influence of parasitic capacity of PD effectively, it is demanded that the input impedance of TIA should be designed as small as possible.

As illustrated in Figure 1, the input stage employs the configuration of enhancement type regulated cascade (ETRGC), and it consists of three stages of voltage gain of A_1, A_2 and A_3. The A_1, A_2 and A_3 is the voltage gain of input node to source of M_6, source of M_6 to gate of M_1, and gate of M_1 to output, respectively, which can reduce the input impedance effectively and ensure a sufficient gain and bandwidth. The transimpedance gain Z_{TIA} can be approximated as follows [1–3]:

$$Z_{\mathrm{TIA}} = \frac{Z_{\mathrm{out}}}{1 + sC_{\mathrm{i,total}} Z_{\mathrm{out}} / A_1 A_2 A_3}, \tag{1}$$

where Z_{out} is the output impedance, and $C_{\mathrm{i,total}}$ is the total input capacity.

From the (1), it can be seen that the bandwidth can be expanded effectively by enlarging the voltage gain of A_1, A_2 and A_3. To further improve the bandwidth, a structure of active inductor as shown in Figure 2 is also employed. The equivalent model of active inductor is shown in Figure 2. Ignoring second effects, the equivalent output impedance and equivalent inductance can be expressed as follows[4]:

$$Z_{\mathrm{out}} = \frac{1 + sR_{\mathrm{g}}C_{\mathrm{gs}}}{g_{\mathrm{m}} + sC_{\mathrm{gs}}}, \tag{2}$$

$$L = \frac{C_{\mathrm{gs}}}{g_{\mathrm{m}}} \left(R_{\mathrm{g}} - 1/g_{\mathrm{m}}\right). \tag{3}$$

As shown in (2), $|Z_{\mathrm{out}}|$ increases with frequency and behaves as an inductor. According to the PVT analysis, the $|Z_{\mathrm{out}}|$ can retain inductive with the appropriate value of R_{g} and $1/g_{\mathrm{m}}$. Thus, the bandwidth of input stage is further improved by this inductive load.

2.2 Gain stage

As the second stage of TIA, the gain stage is proposed to further enlarge the signal generated by input stage. To ensure the demand of bandwidth, the three-order interleaving active feedback configuration is shown in Figure 3. Assume each node has a load of $R_{\mathrm{L}}//(1/sC_{\mathrm{L}})$, the transfer function is given by [5]:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}(s) = -\frac{A^3(s)}{1 + 2A^2(s) A_{\mathrm{f}}(s)}, \tag{4}$$

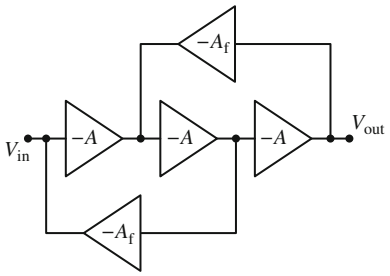


Figure 3 Architecture of three-order interleaving active feedback.

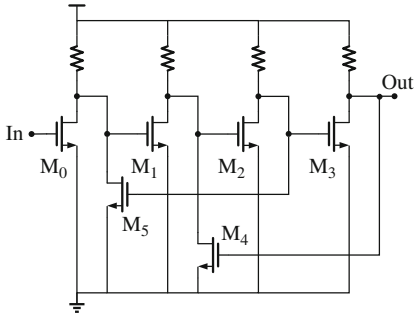


Figure 4 Circuit of three-order interleaving active feedback.

where $A(s) = A/(1 + s/\omega_0)$, $A_f(s) = A_f/(1 + s/\omega_0)$, $\omega_0 = R_L C_L$. A and A_f are the voltage gain of feed-forward and feedback path respectively.

By substituting $A(s)$ and $A_f(s)$ into transfer function, three poles are obtained as follows:

$$\omega_{p1} = -\omega_0\Big(1 + \sqrt[3]{2A^2A_f}\Big), \tag{5}$$

$$\omega_{p2,3} = -\omega_0\Big(1 - \frac{1}{2}\sqrt[3]{2A^2A_f} \pm \mathrm{j}\frac{\sqrt{3}}{2}\sqrt[3]{2A^2A_f}\Big). \tag{6}$$

It is seen that by using three-order interleaving active feedback, the poles of the transfer function has been greatly postponed by A_f, thus the bandwidth is enlarged.

Figure 4 shows the circuit of three-order interleaving active feedback. The M_1, M_2 and M_3 are feed-forward common source amplifiers, and the M_4 and M_5 constitute feedback path.

To reduce the total integrated noise, the bandwidth of the TIA must be minimized, but the limited bandwidth introduces intersymbol interference (ISI) in random data. (7) denotes the relationship between the bandwidth and the produced across-zero jitter:

$$\frac{T_1 - T_2}{T_b} \approx \frac{R_b}{2\pi f_{-3dB}} \exp\left[\frac{-2\pi f_{-3dB}}{R_b}\right], \tag{7}$$

where T_b represents the period of the data streams, $T_1 - T_2$ is the across-zero jitter and R_b denotes the bit rate of the data streams. If $f_{-3dB} = 0.5R_b$, then the jitter is 1.38%; and if $f_{-3dB} = 0.7R_b$, the jitter decreased to 0.28%. The trade-off between noise and ISI appears to improve as the bandwidth goes from $0.5R_b$ to $0.7R_b$ [6]. In this design, $0.8R_b$ is chosen because actual circuits may contain more poles, in addition technology and temperature variations mandate additional margin.

3 LA design

LA is proposed to amplify the voltage signal from TIA to a certain amplitude to meet the need of follow-up clock and data recovery circuit (CDR). LA is constructed by the input buffer, the five broadband-amplify core cells and the output buffer. Noting that the final output is a limiting signal, the last stage should be worked in large signal state.

As the input buffer of LA, it has to convert the single end signal from TIA to differential signal to meet the need of follow-up. At the same time, there exists DC offset in practical circuit for the reason of unmatched, which means the input buffer has a task of DC offset cancellation. The circuit of the input buffer is shown in Figure 5. High-frequency signal and the DC level extracted by RC low-pass filter are sent to a differential amplifier, which realizes single-to-differential conversion. On the other hand, the extracted DC component from the signal between five broadband-amplify cells and output buffer is sent to input buffer, thus achieves the function of DC offset cancellation.

The architecture of the core circuit is shown in Figure 6, the core circuit of LA is composed of five broadband amplify cells. The front four cells employ three-order interleaving active feedback architecture,

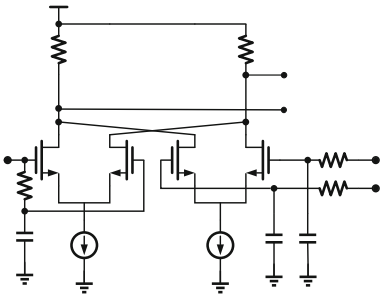


Figure 5 Circuit of input buffer.

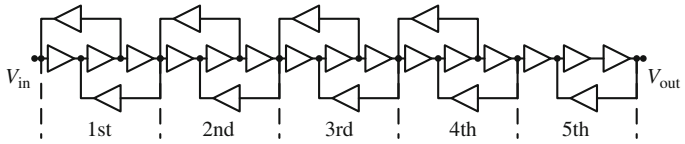


Figure 6 Architecture of core circuit of LA.

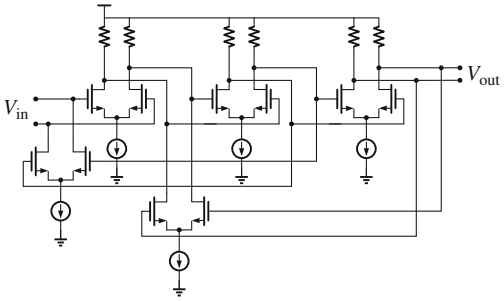


Figure 7 Circuit of the front four cells.

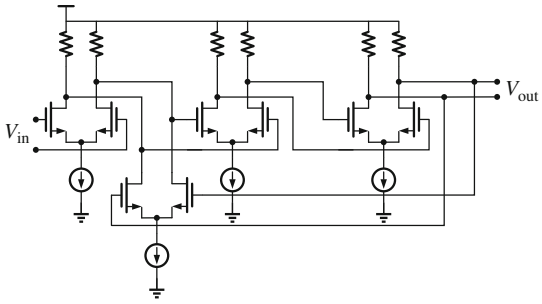


Figure 8 Circuit of the fifth cell.

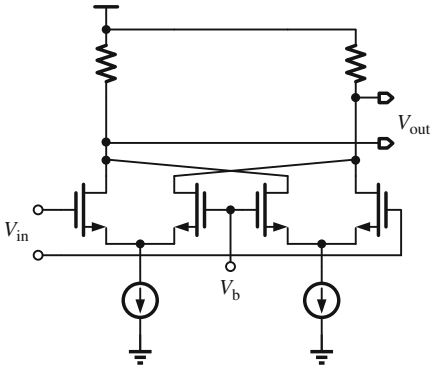


Figure 9 Circuit of output buffer.

similar to the gain stage of TIA [7–9]. Noting that the signal in LA is differential, the amplify cells are realized in differential form correspondingly. The circuit of the front four cells and the fifth cell are shown in Figure 7 and Figure 8 respectively. To obtain a better large signal characteristic, the fifth cell employs traditional three-order active feedback, instead of the interleaving one.

An output buffer is usually required in LA as well as FEA. As shown in Figure 9, the output buffer adopts a structure of dual f_T. This structure can put the input gate capacitances C_{GS} of two input transistors in series to reduce the C_{GS} into half [10], thus increasing the speed of output buffer drastically.

4 Simulation and experimental results

The 4-channel parallel 40 Gb/s front-end amplifier is designed in TSMC 0.18 μm CMOS technology. The layout of each 10 Gb/s channel grid has a pitch of 250 μm. To suppress the substrate and supply coupling noise from adjacent channels, each channel is surrounded by two P+ and N well guard rings. The P+ guard ring is connected to ground and the N well guard ring is connected to power supply, this reverse biased pn junction can suppress the substrate and supply coupling noise significantly. Assuming the parasitic capacitance of PD and the input bondiong PAD of the layout is 200 fF, the simulated frequency

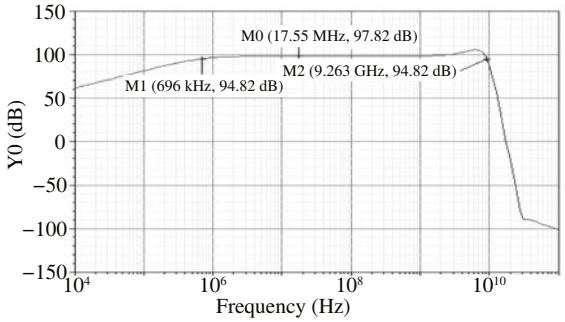


Figure 10 The simulated gain-bandwidth response of the FEA.

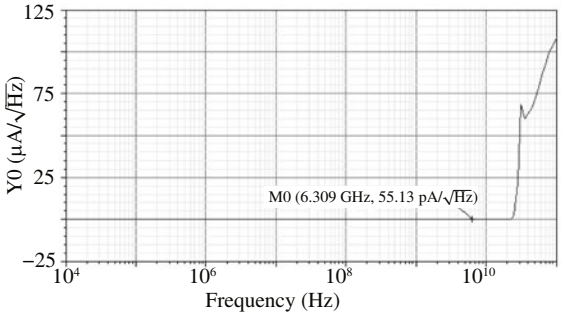


Figure 11 The equivalent input noise current of the FEA.

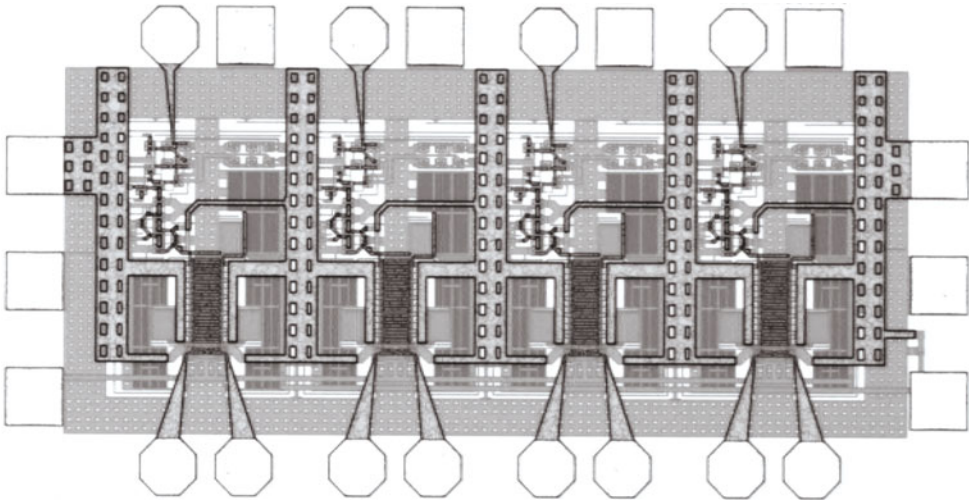
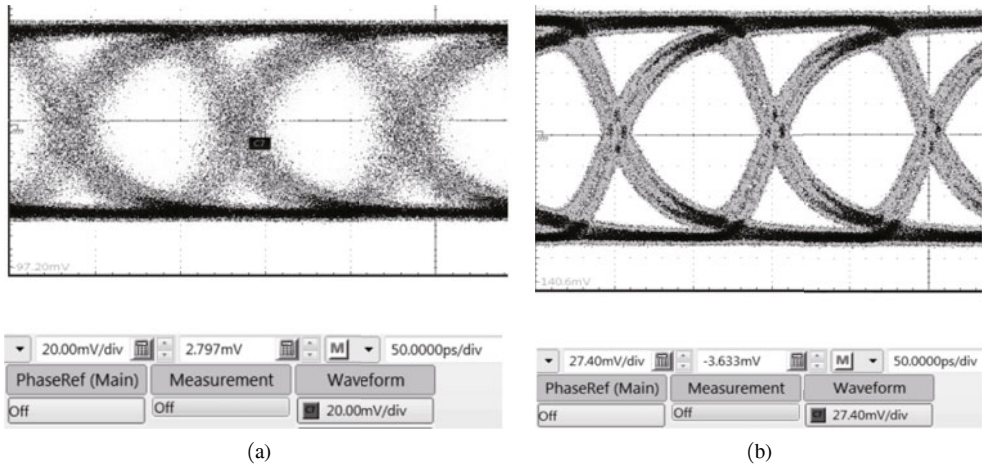


Figure 12 Micrograph of 4-channel parallel 40 Gb/s FEA.



(a) (b)

Figure 13 10 Gb/s eye diagram with the input swing of (a) 5 mV_{pp}; (b) 500 mV_{pp}.

response of the TIA and LA is shown in Figure 10 and the −3 dB bandwidth is 9.26 GHz. The equivalent input noise current spectral density of the FEA is 55.13 pA/$\sqrt{\text{Hz}}$ as shown in Figure 11. The micrograph of the 40 Gb/s FEA chip is shown in Figure 12 and it occupies an area of 650 μm × 1300 μm.

The measured output eye diagrams of a single FEA channel with differential outputs at 10 Gb/s with 5 mV and 500 mV is shown in Figure 13(a) and Figure 13(b), respectively. Considering the input impedance is 50 ohm, so the FEA exhibits a sensitivity of 100 μA input current. The maximum 12 Gb/s

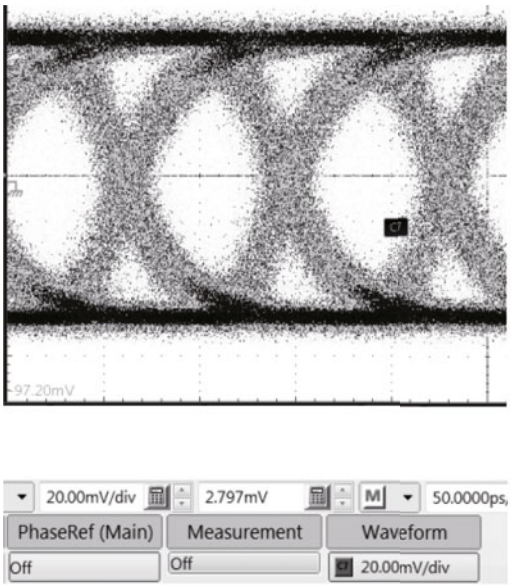


Figure 14 12 Gb/s eye diagram with the input swing of 20 mV_{pp}.

Table 1 Performance comparison with other works

Design	Ref. [11]	Ref. [12]	This work
Function	TIA+LA	TIA	TIA+LA
Technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Maximum channel rate (Gb/s)	10	40	12
Bandwidth (GHz)	7.6	30.5	9.3
C_{pd} (fF)	150	50	200
Sensitivity	−12 dBm	135.8 μA	100 μA
Gain (dBΩ)	87	51	98
Output swing	400		210 mV
Inductor counts	8	15	0
Area (mm×mm)	1.028 × 1.796	1.17 × 0.46	0.65 × 0.325
Power (mW)	210	60.1	92 mW per channel

output eye diagram of the single FEA channel is shown in Figure 14. The output eye diagram maintains stable and clear with a limiting range of output voltage of 210 mV_{pp} on 50 Ω load.

The circuit performance comparison of this 40 Gb/s front-end amplifier and prior works [11,12] is summarized in Table 1. The proposed inductorless FEA is power, cost, and area efficient for the 40 Gb/s parallel optical fiber communication systems.

5 Conclusions

This paper proposed a single-chip optical receiver front-end amplifier array for 40 Gb/s parallel optical transmission systems in a standard TSMC 0.18 μm CMOS technology. A novel enhancement type regulated cascade (ETRGC) configuration with an active inductor has been contrived in this paper for the TIA to broaden the bandwidth. The technique of three-order interleaving active feedback expands the bandwidth of the gain stage of TIA and LA. The experimental results show that the entire front-end amplifier has a large dynamic range, low power consumption and low cost, which is suitable for high-speed parallel data transmission.

Acknowledgements

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