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Principle of designing slope compensation in PFC Boost converter

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Due to wide input fluctuation with line frequency of 50 Hz, power-factor-correction (PFC) Boost converters tend to exhibit fast-scale instability over time domain. The traditional remedy is to impose slope compensation so as to weaken or eliminate this instability. A theoretical principle on the implementation of slope compensation signal is still lacking. Empirical design will induce over compensation frequently, resulting in a large decrease of power factor. In order to tackle this issue, by constructing the discrete-time iterative map of the PFC Boost converter from the viewpoint of bifurcation control theory of nonlinear systems, consequently, the criterion of critical stability for the PFC circuit can be established. Based on this stability criterion, appropriate design of slope compensation can be achieved. Our work indicates that 3 main circuit parameters (i.e. switching cycle, output reference voltage and inductor) determine the effective amplitude design of the slope compensation signal. The results, validated by a large quantity of analytical and numerical studies, show that appropriate slope compensation can be effective in weakening (or controlling) fast-scale bifurcation while maintaining a rather high input power factor.

PFC Boost converter, peak current mode control, slope compensation, fast-scale bifurcation, bifurcation control

1 Introduction

In the early applications of switching power supply, the AC line voltage was rectified using four-diode bridge, afterwards it was filtered with large capacitor. The power supply absorbs energy from AC power line with a high-amplitude pulse-like current, and it will decrease its efficiency and restrict the development of large switching power supply. Meanwhile, it will also bring higher subharmonic pollution into AC power line. For these reasons, a remedy is shaping the input current of power supply to a sine wave with the same phase angle as AC line voltage, thus achieve the unity power factor. That is to say, inspecting from the AC power line, the power supply can emulate a resistor. With this resistor emulator consideration, many power factor correction circuits are developed. Nowadays, active power factor correction converters serve as a pre-regulator of switching power supplies, owing to its excellent characteristics in volume, cost and performance[1−3].

In most implementations of active power factor correction, usually the Boost converter is the best

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choice of circuit topology[1−3]. In order to obtain nearly unity power factor, and also to achieve tight regulation of output voltage, input current shaping techniques with multiplier as the core are developed, such as peak current mode control, average current mode control, etc. However, because the large fluctuation of AC line voltage, the Boost converter tends to exhibit fast-scale instability[4−12]. The conventional measure is to adopt slope compensation so as to weaken or even eliminate this fast-scale instability[1−3]. But in the practical application, the compensating slope is designed experientially, and over compensation can arise unpredictably. The consequence of over compensation is an increase of the THD (total harmonic distortion) of input current, which will also definitely decrease the power factor of the circuit. Owing to the above reason, in this paper we will carry out theoretical analysis for slope compensation in peak current mode controlled PFC Boost converter based on the bifurcation theory of nonlinear system, and explain the mechanism of designing slope compensation from the bifurcation control viewpoint. Accordingly, we achieve the general design principle ensuring stable operation and simultaneously maintaining high power factor for PFC circuit.

2 Peak current mode controlled PFC Boost converter

The circuit schematic diagram of peak current mode controlled PFC Boost converter is shown in Figure 1(a)[1−5]. The closed loop of the system includes two control parts, outer voltage loop and inner current loop. The voltage loop can provide reference current for inner current loop. In order to control fast-scale instability in PFC converter, the circuit imposing compensation signal $i_{\rm c}$ (in traditional design, the compensation signal is a sawtooth waveform, or sometimes named slope signal), i.e. a compensated reference current $\tilde{i}_{\rm ref}$, is obtained by subtracting $i_{\rm c}$ from the original reference current $i_{\rm ref}$ of the outer voltage loop. In the operation regime of the circuit, the switch $G_{\rm S}$ is turned on with the clock pulse arriving, inductor current will increase consequently; when the inductor current reaches $\tilde{i}_{\rm ref}$, $G_{\rm S}$ is turned off with the inductor current decreasing until the next clock pulse arrives. The reference current $i_{\rm ref}$ is usually the sinusoidal modulation of output voltage error (i.e. multiplying voltage error with rectified input voltage $v_{\rm in}$), therefore the peak of inductor current can follow the sine waveform of input line voltage, and the PFC circuit can obtain a nearly unit power factor.

The main circuit of Boost converter is a second order circuit, including an inductor L, a switch $G_{\rm S}$, a diode $G_{\rm D}$, a capacitor C, and a load R. As the Boost converter operates in DCM (Discontinuous Conduction Mode) when it is used for PFC intention, there are three switch states during one switching cycle, i.e. 1) switch $G_{\rm S}$ turns on, diode $G_{\rm D}$ turns off; 2) switch $G_{\rm S}$ turns off, diode $G_{\rm D}$ turns on; 3) both switch $G_{\rm S}$ and diode $G_{\rm D}$ turn off. The state equations corresponding to these switch states are generally given by

$$\begin{aligned} \dot{x} &= A_1 x + B_1 E \quad \text{switch } G_{\rm S} \text{ on, } G_{\rm D} \text{ off,} \\ \dot{x} &= A_2 x + B_2 E \quad \text{switch } G_{\rm S} \text{ off, } G_{\rm D} \text{ on,} \\ \dot{x} &= A_3 x + B_3 E \quad \text{switch } G_{\rm S} \text{ off, } G_{\rm D} \text{ off,} \end{aligned} \tag{1}$$

where x is the state vector defined as $x = [i_{\rm L} \;\; v_{\rm o}]^{\rm T}$, and coefficient matrix A's and B's are given by

$$\begin{aligned} A_1 = A_3 &= \begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix}, \\ A_2 &= \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}, \\ B_1 = B_2 &= \begin{bmatrix} 1/L \\ 0 \end{bmatrix}, B_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \end{aligned} \tag{2}$$

The above state equations, in conjunction with the voltage-loop and current-loop control in Figure 1(a), will be used in the simulation study. An "exact" cycle-by-cycle simulation can be performed based on SIMULINK, including CCM (continuous conduction mode) and DCM operation. Actually the Boost converter mainly operates in CCM, except minor region of DCM where inductor current crosses zero. Therefore, in our following theoretical analysis, only two switch states (i.e. first two occasions in eq. (1)) are considered.

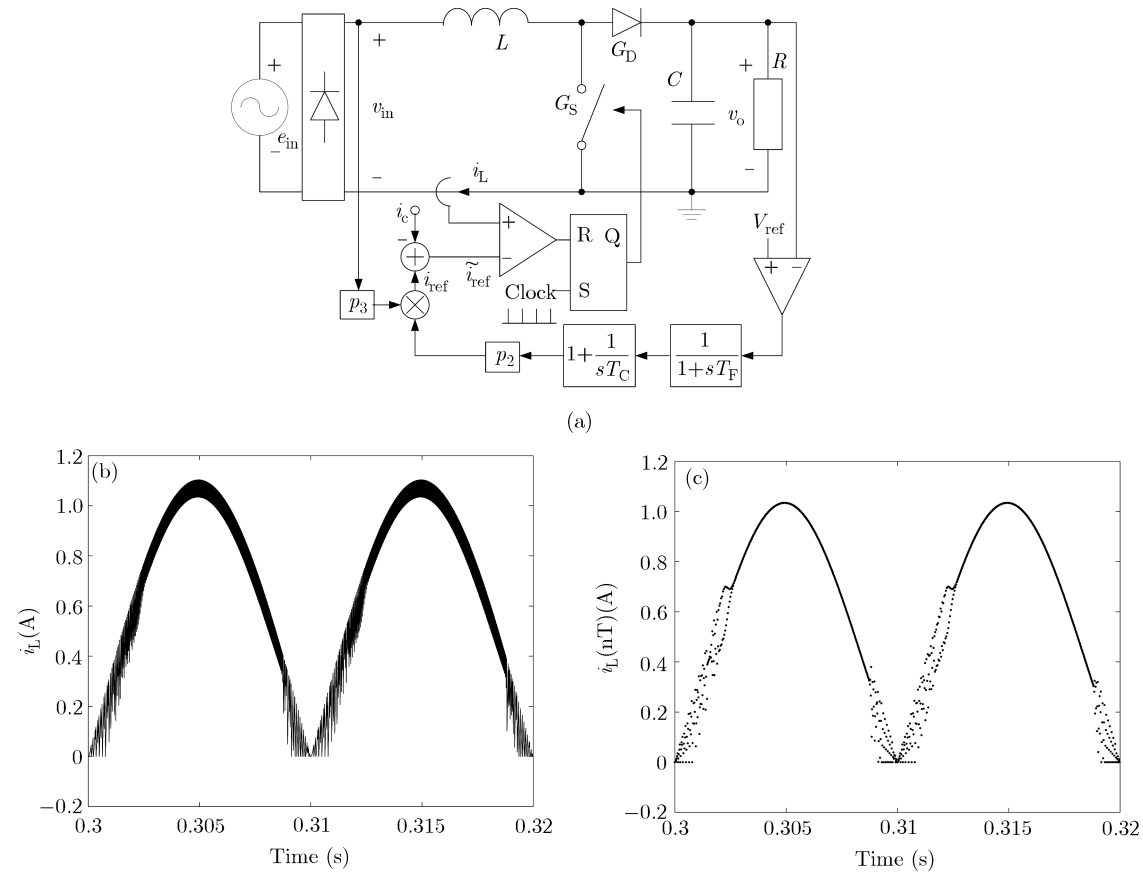

Figure 1 Peak current mode controlled PFC Boost converter. (a) Schematic diagram; (b) time-domain waveform of inductor current; (c) stroboscopically sampled waveform of inductor current.

3 Fast-scale bifurcation in peak current mode controlled PFC Boost converter and its stabilization

3.1 Fast-scale instability

The input e_{in} of the circuit, coming from AC power line, is rectified into the input voltage v_{in} of Boost converter:

$$v_{in} = \hat{V}_{in}|\sin(\omega_m t)| = \hat{V}_{in}|\sin\theta_m|. \quad (3)$$

where $\omega_m = 2\pi f_m$, f_m is line frequency, $\hat{V}_{in}$ is the peak voltage of input power line, θ_m is phase angle. When there is no compensation, i.e. $i_c = 0$, owing to the wide fluctuation of input voltage, inevitably there exists in PFC Boost converter an operation occasion of duty ratio D larger than 0.5[4,13,14], accordingly resulting in fast-scale instability. We carry out the accurate transient simulation based on the parameter selection (Table 1), and then obtain the time domain waveform and stroboscopically sampled waveform of the inductor current as shown in Figure 1(b) and (c). The converter shows two bifurcation branches of the left and right sides during half line period of 0.01 s, and these two bifurcation branches display asymmetry owing to the time-varying characteristic of the reference inductor current.

Table 1 Circuit parameters

Circuit variables	Values
Input voltage e_{in}	22 V RMS
Inductance L	2 mH
Capacitance C	470 μF
Load R	100 Ω
Switching frequency f_s	50 kHz
Switching period T_s	20 μs
Line frequency f_m	50 Hz
Reference voltage V_{ref}	40 V
Feedback gain p_2	1/60
Gain p_3	0.08
Time constant T_F of the filter	4 ms
Time constant T_C of the PI controller	20 ms

3.2 Use of slope compensation in suppression of fast-scale bifurcation

In order to suppress the fast-scale bifurcation discussed in section 3.1, a slope compensation method is adopted in traditional circuit design of Boost converter (i.e. compensation signal in Figure 1(a) is a sawtooth waveform), so the compensated reference current will be

$$\tilde{i}_{\rm ref} = i_{\rm ref} - i_{\rm c} = i_{\rm ref} - S_{\rm ramp}(t \mod T_{\rm s}),$$

where $S_{\rm ramp}$ is the slope of the sawtooth waveform. Whereas there exists experimentalism while the slope compensation method is implemented in an actual circuit design, which will result in an increase of THD in inductor current if the over compensation is employed improperly. The situation can be explained with Figure 2. In contrast to the case of employing appropriate compensation in Figure 2(a), Figure 2(b) gives the case of employing over compensation. From Figure 2(b) we can see that the peak inductor current deviates far away from the sinusoidal reference current $i_{\rm ref}$, with the consequences of remarkable increase of distortion in the average inductor current, and negative influence on the input power factor of the converter.

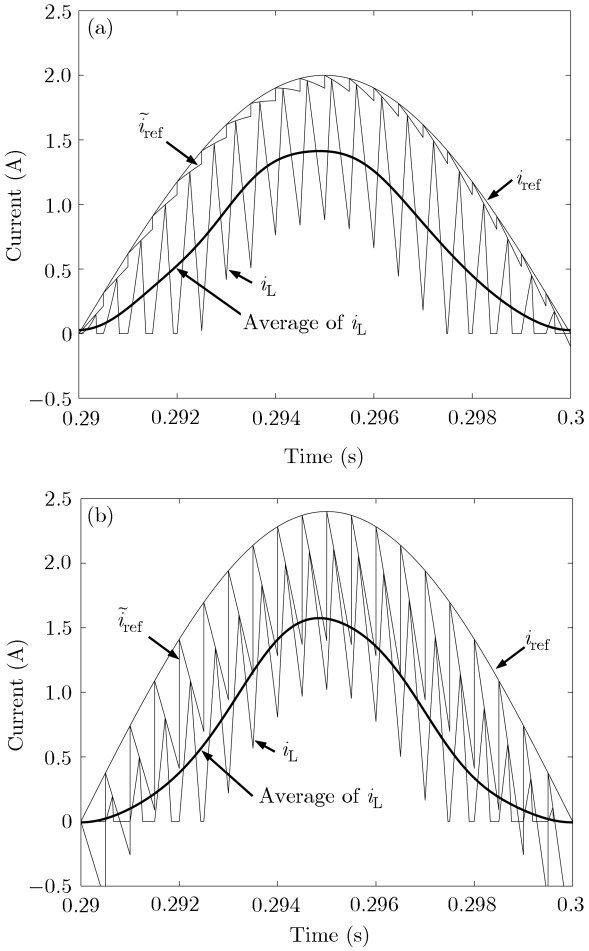

Figure 2 Illustration of slope compensation for fast-scale bifurcation. (a) Appropriate slope compensation; (b) over slope compensation.

4 Analysis of slope compensation in suppression of fast-scale bifurcation

4.1 The mechanism of applying slope compensation to inductor current for suppressing fast-scale instability

Recent researches indicate that the slope compensation, which suppresses fast-scale instability in Boost DC-DC converter, can be explained as a means of bifurcation control method[13,14]. So we can implement analysis from the nonlinear system viewpoint, and expand this theoretical analysis similarly to the analysis of PFC converter.

The PFC Boost converter can be regarded as a series of DC-DC Boost converters over continuous time moments. For every moment, the input voltage of the DC-DC Boost converter is constant. Based on these considerations, we can study PFC Boost converter from the viewpoint of compensation to reference current, i.e."any periodic signal with a positive slope can be treated as a bifurcation control that aims to enhance the stability of the converter, while any periodic signal with a negative slope can be used as a bifurcation anti-control that reduces the stability of the converter."[13] For our research object of PFC Boost converter, there are two compensation sources. The first compensation comes from the slope of multiplier of 50 Hz AC line voltage, and the second is introduced by imposed slope compensation signal. In order to design an appropriate compensation signal for suppressing fast-scale bifurcation and avoiding the over compensation illustrated in subsection 3.2, in this subsection we will make a complete study of applying slope compensation to reference current, and give the analysis to the constructed discrete iterative map of the converter based on the bifurcation theory, hereafter derive the theoretical design

principle for slope compensation.

While the slope compensation is applied to the control of fast-scale bifurcation, the key operational waveforms are illustrated in Figure 3. During one switching cycle, switch $G_{\rm S}$ is turned on firstly by the clock pulse, leading to the increase of inductor current; then off according to the output of a comparator that compares the inductor current $i_{\rm L}$ with the compensated reference current $\tilde{i}_{\rm ref}$, with the consequence of decrease of inductor current. So we can conclude the relationship of the stroboscopically sampled inductor current $i_{\rm n}$ and $i_{\rm n+1}$ as

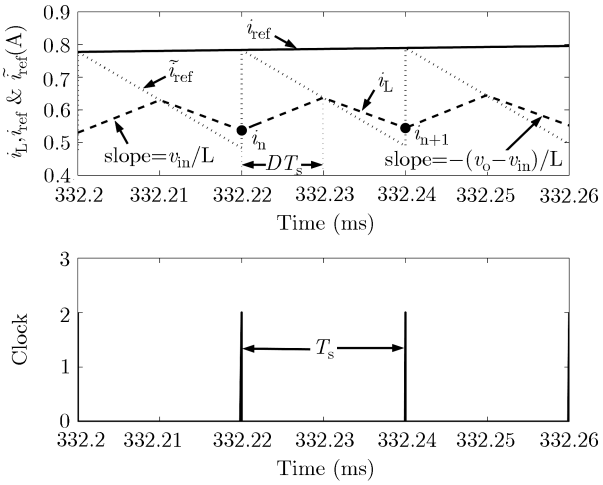

Figure 3 Operational mechanism of slope compensation.

$$\begin{cases} \dfrac{\tilde{i}_{\rm ref}-i_{\rm n}}{DT_{\rm s}}=\dfrac{\hat{V}_{\rm in}\sin(\omega_{\rm m}t)}{L}, \\ \dfrac{\tilde{i}_{\rm ref}-i_{\rm n+1}}{(1-D)T_{\rm s}}=\dfrac{v_{\rm o}-\hat{V}_{\rm in}\sin(\omega_{\rm m}t)}{L}, \end{cases} \tag{4}$$

where $\tilde{i}_{\rm ref}=i_{\rm ref}-i_{\rm c}=\hat{I}_{\rm ref}\sin(\omega_{\rm m}t)-i_{\rm c}$. Also considering $t=nT_{\rm s}+DT_{\rm s}$ at the moment of $G_{\rm S}$ turning off, we can get

$$\begin{cases} \dfrac{\hat{I}_{\rm ref}\sin[\omega_{\rm m}(nT_{\rm s}+DT_{\rm s})]-i_{\rm c}(nT_{\rm s}+DT_{\rm s})-i_{\rm n}}{DT_{\rm s}}=\dfrac{\hat{V}_{\rm in}\sin[\omega_{\rm m}(nT_{\rm s}+DT_{\rm s})]}{L}, \\ \dfrac{\hat{I}_{\rm ref}\sin[\omega_{\rm m}(nT_{\rm s}+DT_{\rm s})]-i_{\rm c}(nT_{\rm s}+DT_{\rm s})-i_{\rm n+1}}{(1-D)T_{\rm s}}=\dfrac{v_{\rm o}-\hat{V}_{\rm in}\sin[\omega_{\rm m}(nT_{\rm s}+DT_{\rm s})]}{L}. \end{cases} \tag{5}$$

The perturbed form of eq. (5) is

$$\begin{cases} \dfrac{\hat{I}_{\rm ref}\sin[\omega_{\rm m}nT_{\rm s}+\omega_{\rm m}(D+\delta_{\rm D})T_{\rm s}]-i_{\rm c}[nT_{\rm s}+(D+\delta_D)T_{\rm s}]-(i_{\rm n}+\delta i_{\rm n})}{(D+\delta_{\rm D})T_{\rm s}} \\ \qquad=\dfrac{\hat{V}_{\rm in}\sin[\omega_{\rm m}nT_{\rm s}+\omega_{\rm m}(D+\delta_{\rm D})T_{\rm s}]}{L}, \\ \dfrac{\hat{I}_{\rm ref}\sin[\omega_{\rm m}nT_{\rm s}+\omega_{\rm m}(D+\delta_{\rm D})T_{\rm s}]-i_{\rm c}[nT_{\rm s}+(D+\delta_{\rm D})T_{\rm s}]-(i_{\rm n+1}+\delta i_{\rm n+1})}{[1-(D+\delta_{\rm D})]T_{\rm s}} \\ \qquad=\dfrac{v_{\rm o}-\hat{V}_{\rm in}\sin[\omega_{\rm m}nT_{\rm s}+\omega_{\rm m}(D+\delta_{\rm D})T_{\rm s}]}{L}. \end{cases} \tag{6}$$

We can divide this equation into two parts, i.e. steady and transient state, and consider only the transient variables:

$$\begin{cases} \hat{I}_{\rm ref}\omega_{\rm m}T_{\rm s}\cos\theta_{\rm m}\delta_{\rm D}-S_{\rm ramp}T_{\rm s}\delta_{\rm D}-\delta i_{\rm n}=\dfrac{\hat{V}_{\rm in}T_{\rm s}}{L}(\sin\theta_{\rm m}+\omega_{\rm m}DT_{\rm s}\cos\theta_{\rm m})\delta_{\rm D}, \\ \hat{I}_{\rm ref}\omega_{\rm m}T_{\rm s}\cos\theta_{\rm m}\delta_{\rm D}-S_{\rm ramp}T_{\rm s}\delta_{\rm D}-\delta i_{\rm n+1}=-v_{\rm o}\dfrac{\delta_{\rm D}T_{\rm s}}{L}-\dfrac{\hat{V}_{\rm in}T_{\rm s}}{L}[-\sin\theta_{\rm m}+\omega_{\rm m}DT_{\rm s}\cos\theta_{\rm m}(1-D)]\delta_{\rm D}. \end{cases} \tag{7}$$

Combing the two equations in (7), we obtain the iterative equation of transient inductor current as

$$\delta i_{\rm n+1}=\frac{\hat{I}_{\rm ref}\omega_{\rm m}\cos\theta_{\rm m}-S_{\rm ramp}+\frac{v_{\rm o}}{L}-\frac{\hat{V}_{\rm in}}{L}[\sin\theta_{\rm m}+\omega_{\rm m}(D-1)T_{\rm s}\cos\theta_{\rm m}]}{\hat{I}_{\rm ref}\omega_{\rm m}\cos\theta_{\rm m}-S_{\rm ramp}-\frac{\hat{V}_{\rm in}}{L}(\sin\theta_{\rm m}+\omega_{\rm m}DT_{\rm s}\cos\theta_{\rm m})}\delta i_{\rm n}. \tag{8}$$

Now from eq. (8), we can get the characteristic multiplier λ

$$\lambda=\frac{\hat{I}_{\rm ref}\omega_{\rm m}\cos\theta_{\rm m}-S_{\rm ramp}+\frac{v_{\rm o}}{L}-\frac{\hat{V}_{\rm in}}{L}[\sin\theta_{\rm m}+\omega_{\rm m}(D-1)T_{\rm s}\cos\theta_{\rm m}]}{\hat{I}_{\rm ref}\omega_{\rm m}\cos\theta_{\rm m}-S_{\rm ramp}-\frac{\hat{V}_{\rm in}}{L}(\sin\theta_{\rm m}+\omega_{\rm m}DT_{\rm s}\cos\theta_{\rm m})}. \tag{9}$$

When λ is located in the stable region $(-1, 1)$, the converter will operate in regular period 1. If λ gets cross this stable region through -1, the converter exhibits period-doubling bifurcation, and gives birth to stable period 2. So $\lambda = -1$ will be the critical condition of period-doubling bifurcation. Based on this, also considering eq. (3) and taking into account the input-output voltage conversion ratio $\frac{1}{1-D} = \frac{V_{\rm ref}}{v_{\rm in}}$, we can get the critical stable expression

$$2\hat{I}_{\rm ref}\omega_{\rm m}\cos\theta_{\rm m} - 2S_{\rm ramp} + \frac{V_{\rm ref}}{L} - \frac{\hat{V}_{\rm in}}{L} \left\{2\sin\theta_{\rm m} + \omega_{\rm m}T_{\rm s}\left[2\left(1 - \frac{v_{\rm in}}{V_{\rm ref}}\right) - 1\right]\cos\theta_{\rm m}\right\} = 0. \quad (10)$$

Finally we put into the power-balance equation $\frac{\hat{V}_{\rm in}\hat{I}_{\rm ref}}{2} = \frac{V_{\rm ref}^2}{R}$, and obtain the slope expression of compensation signal as

$$S_{\rm ramp} = \frac{V_{\rm ref}}{2L} + \frac{2\omega_{\rm m}V_{\rm ref}^2}{R\hat{V}_{\rm in}}\cos\theta_{\rm m} - \frac{\hat{V}_{\rm in}}{L}\left[\sin\theta_{\rm m} + \omega_{\rm m}T_{\rm s}\left(\frac{1}{2} - \frac{\hat{V}_{\rm in}\sin\theta_{\rm m}}{V_{\rm ref}}\right)\cos\theta_{\rm m}\right]. \quad (11)$$

Eq. (11) indicates the compensation signal slope ensuring stability of converter for the critical phase angle $\theta_{\rm m}$. Owing to the time-varying characteristic of AC line voltage, the left critical bifurcation point will always be higher than the right one over half line period (Figure 1(b) and (c)), i.e. the left bifurcation branch exhibits worse stability. So we can make the converter stable over the entire line period by letting critical phase angle be equal to 0. Then eq. (11) becomes

$$S_{\rm ramp} = \frac{V_{\rm ref}}{2L} + \frac{2\omega_{\rm m}V_{\rm ref}^2}{R\hat{V}_{\rm in}} - \frac{\omega_{\rm m}T_{\rm s}\hat{V}_{\rm in}}{2L}. \quad (12)$$

For the slope compensation signal implemented, we can simply calculate its amplitude $A_{\rm ramp}$ with (12):

$$A_{\rm ramp} = T_{\rm s}S_{\rm ramp} = \frac{V_{\rm ref}T_{\rm s}}{2L} + \frac{2\omega_{\rm m}V_{\rm ref}^2T_{\rm s}}{R\hat{V}_{\rm in}} - \frac{\omega_{\rm m}T_{\rm s}^2\hat{V}_{\rm in}}{2L}. \quad (13)$$

Eq. (13) gives the amplitude design principle of slope compensation. In the real engineering application, the last two parts in (13), which are extremely small compared to its first part, can be neglected when evaluating the value for simplicity. Specifically we can find that there are three circuit parameters in the first part of (13), i.e. switching cycle $T_{\rm s}$, reference voltage $V_{\rm ref}$ and inductor L, which make overwhelming influence on the design of slope compensation. The calculated results of $A_{\rm ramp}$ based on (13) are shown in Figure 4 marked with '*', meanwhile we provide the corresponding values of demanded slope amplitude (marked with 'o') obtained from numerical simulations. We find out that the results are consistent, i.e., by increasing switching cycle or output reference voltage, or decreasing inductor, the demanded amplitude of slope compensation signal will increase for guaranteeing stable operation of the converter.

As an example, we give the suppression result (Figure 5) of the fast-scale bifurcation introduced in Figure 1(b) and (c). Though the inductor waveforms in the figure exhibit bifurcation free operation, we should bear in mind that completely ideal compensation is impossible, because theoretical

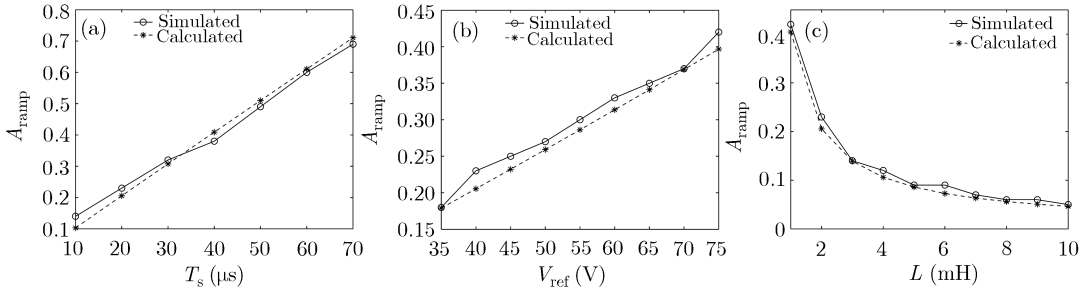

Figure 4 Comparison of simulated and calculated amplitude for appropriate slope compensation with changing of (a) switching cycle $T_{\rm s}$; (b) reference voltage $V_{\rm ref}$; (c) inductor L.

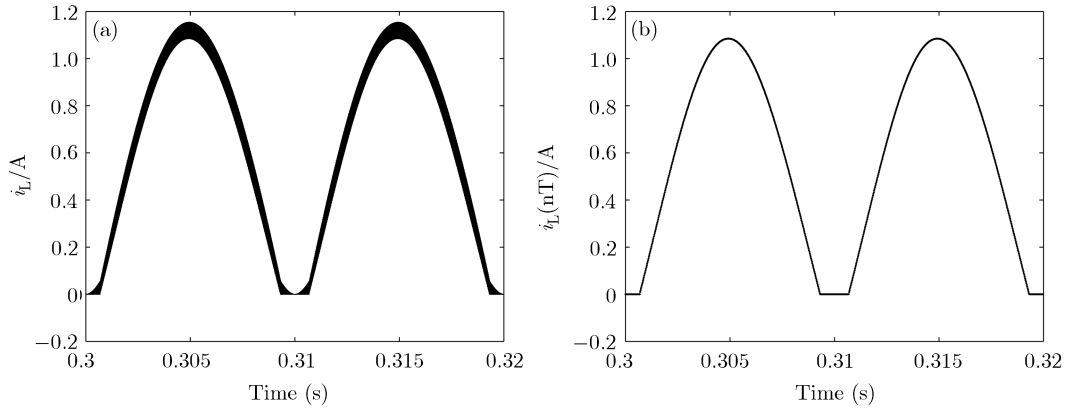

Figure 5 Inductor current waveform under effective slope compensation designed by (13), with parameters in Table 1. (a) Time-domain waveform; (b) stroboscopically sampled waveform.

input-output voltage conversion ratio tends to infinity when inductor current approaches 0. But on this occasion the converter operates in DCM, and the bifurcation is constrained on time axis, and cannot be observed directly. So we approximately regard that fast-scale bifurcation is suppressed.

4.2 Influence of slope compensation on input power factor

As stated before, with the addition of slope compensation the fast-scale bifurcation in PFC Boost converter can be suppressed (or controlled). But simultaneously the average inductor current will deviate further from the standard sine waveform (as illustrated in subsection 3.2), with the consequence of decrease of input power factor. While the theoretical analysis of subsection 4.1 gives an appropriate design principle of slope compensation, which can minimize the negative influence on the power factor to the greatest extent. Figure 6 shows the change of power factor for various circuit parameters, from which we may reach the following conclusions:

1) For the case of no compensation (no comp.), the converter possesses a rather high input power factor through there exists fast-scale bifurcation. But the power factor will decline slightly with switching cycle T_s increasing, reference voltage V_{ref} or inductor L decreasing.

2) For the case where there is an appropriate slope compensation designed as before (appr. slope comp.), the converter can maintain a rather high input power factor, through a bit lower than that of the first case of without compensation.

3) For the case where there is an over slope compensation (over slope comp.) with 5 or 10 times amplitude of appropriate compensation, the converter gives a worse power factor than the former two cases, and will have a far worse power factor with the compensation extent being stronger.

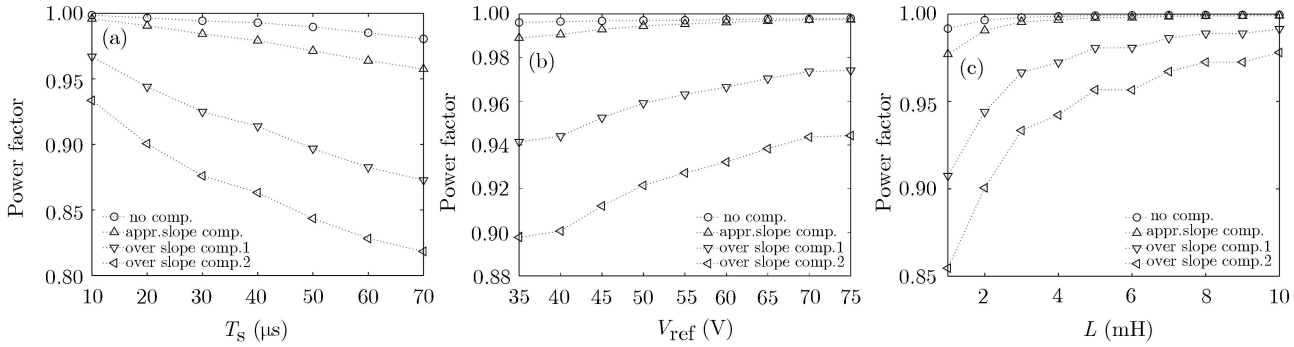

Figure 6 Influence of slope compensation on the power factor with changing of (a) switching cycle T_s; (b) reference voltage V_{ref}; (c) inductor L.

5 Conclusions

Traditional method of slope compensation can weaken (or control) fast-scale bifurcation in PFC converter so as to avoid fast-scale instability. As the design procedure lacks a theoretical basis, as a consequence of inappropriate over compensation, a dramatic decrease of input power factor will be induced. From the bifurcation theory of nonlinear system, we have carried out in this paper the stability analysis for this traditional method of suppressing fast-scale bifurcation based on the slope compensation, and established the general design formulae (12) and (13) of compensation slope signal. The results can achieve the best suppression (or control) on the fast-scale bifurcation commonly existing in PFC converters, and maintain a high input power factor at the same time.

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